UNIVERSIDAD AUTÓNOMA DE BAJA CALIFORNIA

Facultad de Ingeniería Arquitectura y Diseño

Maestría y Doctorado en Ciencias e Ingeniería

MEMRISTORS BASED ON MIXED METAL OXIDES: ELECTRICAL RESPONSE AND EXPLORATION OF SYNAPTIC FUNCTIONALITY

Thesis submitted in partial fulfillment of the requirements for the degree of Master of Engineering.

José Miguel Menchaca Rodríguez

Supervisor:

Dr. Enrique Efrén García Guerrero

Co-Supervisor:

Dr. Hugo Jesús Tiznado Vázquez

JANUARY, 2025

ENSENADA BAJA CALIFORNIA, MÉXICO

UNIVERSIDAD AUTÓNOMA DE BAJA CALIFORNIA

Facultad de Ingeniería Arquitectura y Diseño

Maestría y Doctorado en Ciencias e Ingeniería

MEMRISTORS BASED ON MIXED METAL OXIDES: ELECTRICAL RESPONSE AND EXPLORATION OF SYNAPTIC FUNCTIONALITY

THESIS

To obtain the Master of engineering degree, presents:

Jose Miguel Menchaca Rodriguez

Approved by:

Dr. Enrique Efrén García Guerrero
Supervisor

Dr. Hugo Jesús Tiznado Vázquez
Co-Supervisor

Dr. Oscar Adrián Aguirre Castro
Member of committee

Dr. Everardo Inzunza González
Member of committee

Dr. Ulises Jesús Tamayo Pérez
Member of committee

Dr. Oscar Roberto López Bonilla
Member of committee

Ensenada Baja California, México. December 2025

Abstract of the Jose Miguel Menchaca Rodríguez thesis, submitted in partial fulfillment of the requirement of the degree of MASTER OF ENGINEERING, Ensenada B.C, December 2025.

"MEMRISTORS BASED ON MIXED METAL OXIDES: ELECTRICAL RESPONSE AND EXPLORATION OF SYNAPTIC FUNCTIONALITY"

Approved by:

Dr. Enrique Efrén García Guerrero
Supervisor

Dr. Hugo Jesús Tiznado Vázquez
Co-Supervisor

Abstract: Resistive switching (RS) devices, commonly known as memristors, are key candidates for next-generation non-volatile memory and neuromorphic computing due to their simple metal–insulator–metal (MIM) architecture, scalability, and low power consumption. However, their reproducibility and endurance remain limited by material selection and interfacial control. This thesis work investigates the role of interface engineering through multilayer stacking in metal oxide memristors, focusing on ZnO and Al_2O_3 combinations with various electrode materials (Au, Ru, and ITO). The memristive devices were fabricated using different deposition techniques such as atomic layer deposition (ALD) for the oxide's deposition, sputtering and thermal evaporation for the electrodes. The structures fabricated were: Au/ZnO(10nm)/Al_2O_3(10nm)/Ru, single layer Au/Al_2O_3(20nm)/ITO, Au/ZnO(10nm)/Al_2O_3(10nm)/ITO, and Au/ZnO(10nm)/Al_2O_3(2nm)/ITO. The electrical characterization of the devices included I–V cycling, endurance tests, and statistical Weibull analysis to evaluate the resistive switching performance.

The results obtained revealed that electrode morphology and oxide stacking strongly dictate device behavior. Ruthenium based structures exhibited poor reproducibility, which was attributed to high surface roughness and competing filament nucleation at the ZnO/Al_2O_3 and Al_2O_3/Ru interfaces. In contrast, replacing Ru with ITO significantly improved stability and enabled clear bipolar resistive switching. The Au/ZnO(10nm)/Al_2O_3(10nm)/ITO configuration achieved consistent SET/RESET transitions, though with high high-resistance-state variability (CV ≈ 82%). Reducing the Al_2O_3 barrier to 2nm in the structure yielded forming-free operation, lower switching voltages, and enhanced reproducibility, confirming the critical role of ultrathin interfacial layers in filament confinement and current regulation. Weibull analysis of SET and RESET voltages further quantified improved uniformity and reliability in the optimized bilayer design.

Overall, this work demonstrates that fine tuning of multilayered structures effectively controls resistive switching characteristics and enhances the stability of oxide-based memristors. The insights gained into interface-mediated switching dynamics and variability reduction contribute to advancing memristor design for reliable non-volatile memory and neuromorphic synaptic applications.

Keywords: Memristor, Bilayer memristors, resistive switching, analog switching, ZnO/Al_2O_3 bilayer.

ABSTRACT

Resistive switching (RS) devices, commonly known as memristors, are key candidates for next-generation non-volatile memory and neuromorphic computing due to their simple metal–insulator–metal (MIM) architecture, scalability, and low power consumption. However, their reproducibility and endurance remain limited by material selection and interfacial control. This thesis work investigates the role of interface engineering through multilayer stacking in metal oxide memristors, focusing on ZnO and Al_2O_3 combinations with various electrode materials (Au, Ru, and ITO). The memristive devices were fabricated using different deposition techniques such as atomic layer deposition (ALD) for the oxide's deposition, sputtering and thermal evaporation for the electrodes. The structures fabricated were: Au/ZnO(10nm)/Al_2O_3(10nm)/Ru, single layer Au/Al_2O_3(20nm)/ITO, Au/ZnO(10nm)/Al_2O_3(10nm)/ITO, and Au/ZnO(10nm)/Al_2O_3(2nm)/ITO. The electrical characterization of the devices included I–V cycling, endurance tests, and statistical Weibull analysis to evaluate the resistive switching performance.

The results obtained revealed that electrode morphology and oxide stacking strongly dictate device behavior. Ruthenium based structures exhibited poor reproducibility, which was attributed to high surface roughness and competing filament nucleation at the ZnO/Al_2O_3 and Al_2O_3/Ru interfaces. In contrast, replacing Ru with ITO significantly improved stability and enabled clear bipolar resistive switching. The Au/ZnO(10nm)/Al_2O_3(10nm)/ITO configuration achieved consistent SET/RESET transitions, though with high high-resistance-state variability (CV ≈ 82%). Reducing the Al_2O_3 barrier to 2nm in the structure yielded forming-free operation, lower switching voltages, and enhanced reproducibility, confirming the critical role of ultrathin interfacial layers in filament confinement and current regulation. Weibull analysis of SET and RESET voltages further quantified improved uniformity and reliability in the optimized bilayer design.

Overall, this work demonstrates that fine tuning of multilayered structures effectively controls resistive switching characteristics and enhances the stability of oxide-based memristors. The insights gained into interface-mediated switching dynamics and variability reduction contribute to advancing memristor design for reliable non-volatile memory and neuromorphic synaptic applications.

RESUMEN

Los dispositivos de conmutación resistiva (RS), comúnmente conocidos como memristores, son candidatos clave para la memoria no volátil y la computación neuromórfica de próxima generación debido a su sencilla arquitectura metal-aislante-metal (MIM), su escalabilidad y su bajo consumo energético. Sin embargo, su reproducibilidad y resistencia siguen estando limitadas por la selección de materiales y el control interfacial. Esta tesis investiga el papel de la ingeniería de interfaces mediante el apilamiento multicapa en memristores de óxido metálico, centrándose en combinaciones de ZnO y Al_2O_3 con diversos materiales de electrodo (Au, Ru e ITO). Los dispositivos memristivos se fabricaron utilizando diferentes técnicas de deposición, como la deposición de capas atómicas (ALD) para la deposición del óxido, la pulverización catódica y la evaporación térmica para los electrodos. Las estructuras fabricadas fueron: Au/ZnO(10 nm)/Al_2O_3(10 nm)/Ru, capa única Au/Al_2O_3(20 nm)/ITO, Au/ZnO(10 nm)/Al_2O_3(10 nm)/ITO y Au/ZnO(10 nm)/Al_2O_3(2 nm)/ITO. La caracterización eléctrica de los dispositivos incluyó ciclos I-V, pruebas de resistencia y análisis estadístico de Weibull para evaluar el rendimiento de conmutación resistiva.

Los resultados obtenidos revelaron que la morfología de los electrodos y el apilamiento de óxidos determinan en gran medida el comportamiento del dispositivo. Las estructuras basadas en rutenio mostraron una reproducibilidad deficiente, lo que se atribuyó a la alta rugosidad de la superficie y a la nucleación competitiva de filamentos en las interfaces ZnO/Al_2O_3 y Al_2O_3/Ru. Por el contrario, la sustitución de Ru por ITO mejoró significativamente la estabilidad y permitió una conmutación resistiva bipolar clara. La configuración Au/ZnO (10nm)/Al_2O_3 (10nm)/ITO logró transiciones SET/RESET consistentes, aunque con una alta variabilidad del estado de alta resistencia (CV ≈ 82 %). La reducción de la barrera de Al_2O_3 a 2 nm en la estructura dio lugar a un funcionamiento sin formación, voltajes de conmutación más bajos y una mayor reproducibilidad, lo que confirma el papel fundamental de las capas interfaciales ultrafinas en el confinamiento de los filamentos y la regulación de la corriente. El análisis de Weibull de los voltajes SET y RESET cuantificó aún más la mejora de la uniformidad y la fiabilidad en el diseño optimizado de la doble capa.

En general, este trabajo demuestra que el ajuste fino de las estructuras multicapa controla eficazmente las características de conmutación resistiva y mejora la estabilidad de los memristores basados en óxido. Los conocimientos adquiridos sobre la dinámica de conmutación mediada por la interfaz y la reducción de la variabilidad contribuyen al avance del diseño de memristores para aplicaciones de memoria no volátil fiable y sinápticas neuromórficas.

ACKNOWLEDGMENTS

First, I would like to thank my parents, Mario and Laura, for their endless love and unconditional support, which have made me feel close to them even from afar. I'm deeply grateful to have them in my life and for all their wise advice.

I would also like to thank my girlfriend, Celin, for always being there and making my days better with her kindness and support. She is the light that shines in my life.

Next, I want to thank Dr. Hugo Tiznado for his guidance and support throughout my master's degree. I appreciate his patience, and will be forever grateful for all his teachings, which helped me expand my knowledge and grow as an engineer. I would also like to thank Dr. Efrén García Guerrero for the opportunity to enter the master's program under his supervision and for all of his valuable advice.

I would also like to acknowledge the members of my committee—Dr. Oscar Adrián Aguirre Castro, Dr. Everardo Inzunza González, Dr. Ulises Jesús Tamayo Pérez, and Dr. Oscar Roberto López Bonilla—for their comments and advice, which helped me improve this work.

I would also like to thank and acknowledge the financial support provided by the Secretaría de Ciencia, Humanidades, Tecnología e Innovación (SECIHTI) from 2023 to 2025. This work was made possible by the financial support of DGAPA PAPIIT under project grants IN119023 and IG100925.

Last but not least, I would like to thank the Universidad Autónoma de Baja California, the program of Maestría y Doctorado en Ciencias e Ingeniería, and the Centro de Nanociencias y Nanotecnología, for giving me the opportunity to study here and providing me with the necessary tools.

DEDICATION

This work is dedicated to my parents, Jose Mario Menchaca Ramirez and Laura Enedina Rodriguez Vargaz, for always supporting me in every moment of my life and teaching me to be persistent and to follow my dreams. I also dedicate this work to my sister, Abril Mariana Menchaca Rodriguez, for being the best sister anyone could ask for.

This work is also dedicated to my girlfriend, America Celin Vizairo Tellez, for always encouraging me to think before acting and for embracing me with her love and kindness, which made me believe that there are still truly good people in this world.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1. INTRODUCTION

Memristors, often associated with resistive random-access memories (RRAM), are two-terminal electronic devices that exhibit changes in electrical resistance in response to specific electrical stimuli. Typically fabricated using metal/insulator/metal (MIM) structures as shown in Fig. 1, these devices can alter their resistance when voltages are applied across the electrodes, enabling data storage. The change in conductivity is driven by a combination of physical effects, such as ion migration and filament formation, as well as chemical effects like redox reactions within the insulator layer [1].

The memristor concept was first theorized by Leon Chua in 1971 as the fourth fundamental passive circuit element [2]. Based on symmetry arguments, Chua proposed that the memristor establishes a direct relationship between the electrical flux (the time integral of voltage) and electric charge [3]. In other words, the resistance of the device depends on the total charge that has passed through it. As a result, memristors can store information without requiring energy to maintain the data, making them inherently non-volatile [4].

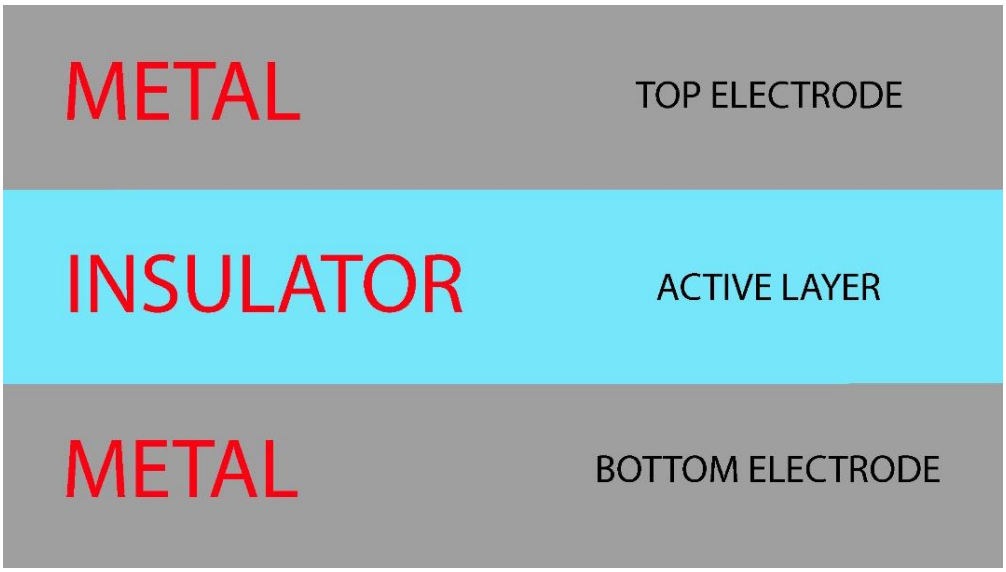

Fig. 1 | Schematic representation of the structure of a memristor device in a MIM configuration

Although the theory of memristive switching was introduced in the 1970s, it was not until 2008 that the first practical demonstration was achieved at HP Laboratories were Stanley Williams and his team observed the memristive behavior at the nanoscale using a TiO_2 film as the active switching layer [5]. Their device exhibited data storage and logic processing capabilities with good retention time, non-volatility, and low power consumption, which highlights the potential of memristors for future computing systems. Despite their compelling characteristics—such as high scalability, multi-level resistive states, low energy consumption, and fast switching speeds—the development of memristive devices still encounters significant challenges. One primary issue is the high variability of the resistive switching parameters, which is intrinsic to thin-film memristors. This variability arises from different factors such as stochastic ion migration and material inhomogeneities, resulting in inconsistent SET/RESET voltages, ON/OFF ratios, and drift among the resistive states.

Additionally, problems related to reliability and endurance, especially under multiple switching cycles, hinder their practical implementation [6]. The resistive switching phenomenon has been observed in various materials, including binary metal oxides, perovskites, chalcogenides, and 2D materials. The switching properties—such as SET/RESET voltages, switching speeds, endurance, and power consumption—are strongly influenced by the materials selection [7]. The resistive switching mechanisms can be broadly classified into five categories based on the underlying physical processes: redox-based RRAM, electrochemical metallization memory (ECM), valence change memory (VCM), thermochemical memory (TCM), and phase change memory (PCM).

1. **Redox-based RRAM:**
   These devices rely on the transport of ions. The switching is achieved through redox reactions that modulate the conductive paths, modifying the device's resistance.
2. **Electrochemical Metallization Memory (ECM):**
   ECM devices utilize reversible electrochemical reduction and oxidation of metallic ions to form and dissolve conductive filaments, thereby altering the resistive state.
3. **Valence Change Memory (VCM):**
   VCM devices operate by altering the oxidation state of the material which changes the electronic structure and conductivity of the active layer.
4. **Thermochemical Memory (TCM):**
   TCM devices depend on localized heating that induces ion migration or phase transitions, which modifies the resistive state.
5. **Phase Change Memory (PCM):**
   PCM devices are based in reversible phase transitions between crystalline and amorphous states, where the crystalline phase exhibits low resistance and the amorphous phase shows high resistance.

This classification highlights the diversity of mechanisms found in memristive devices, supporting applications that span from non-volatile memories to neuromorphic computing. While significant progress has been made, still remain some challenges achieving consistent and reliable operation of memristors, particularly in large-scale arrays. Variability in switching parameters, degradation of the active layer, and electrode deterioration are the major obstacles. To address these issues, research trends have focused on several strategies:

1. **Material Engineering:**
   Optimizing the device's structure using dopants or composite materials, can improve the electrical performance and modulate ion migration.
2. **Device Architecture Optimization:**
   Advanced design of the memristors, such as implementing multilayered structures and using buffer layers, can enhance device's stability and reduce material degradation.
3. **Control of Operating Conditions:**
   Fine-tuning of the operating parameters such as the applied voltages, current compliance (CC), and switching speed helps reducing device's electrical variability and extend device's lifetime.
4. **Modeling and Simulation:**
   Building accurate predictive models of the device's operation can help understanding the resistive switching mechanisms involved and provides a framework for engineering more reliable devices.

Metal-oxide memristors, in particular, have shown high compatibility with CMOS technology and exhibit resistive switching predominantly based on the valence change mechanism (VCM). However, the stochastic migration of oxygen vacancies and uncontrolled oxygen exchange with the electrode materials in the device's structures present significant challenges. Recent advances in multilayer architectures, for the most part through stack engineering, have been promising in stabilizing the switching behavior, enhancing uniformity, and improving the overall performance of RRAM devices.

1.1 Objectives

1.1.1 General objective

The primary objective of this thesis work is to investigate the impact of interface engineering through the multilayer stacking of active layer materials on the enhancement of resistive switching properties in memristors for neuromorphic applications, such as emulating the biological synapse.

1.1.2 Specific objectives

- Synthesize and characterize memristors made of different metal oxides to evaluate and compare their electrical responses, reproducibility, endurance, and explore their potential for emulating the biological synapse.
- Synthesize and characterize multilayered metal oxide memristors to evaluate and compare their electrical response, reproducibility, endurance and explore their potential for emulating the biological synapse.
- Adjust the dielectric layer thickness to assess its impact in the device's electrical performance and its resistive switching behavior.

1.2 Hypothesis

The resistive switching properties of memristors can be improved by multilayer stacking the active layer materials of the device structure, rather than fabricating memristors with a single layer of active materials. Using multilayered structures can make memristors more suitable for emulating biological synapses and in memory computing applications.

CHAPTER 2. STATE OF THE ART

Resistive switching (RS) devices, commonly known as memristors, are recognized for their potential in next-generation non-volatile memory and neuromorphic computing. Their simple metal-insulator-metal (MIM) structure enables scalable fabrication while presenting fast switching, multi-level resistance states, and low-power operation. Despite these advantages, properties such as reproducibility, endurance, and reliability of memristors remain strongly dependent on the selection of the device's electrode and oxide materials, as well as the engineering of interfaces and multilayered structures. This chapter reviews the state of the art surrounding the materials used in the devices of this thesis—Au/ZnO(10nm)/Al_2O_3(10nm)/Ru, Au/Al_2O_3/ITO, bilayer Au/ZnO(10nm)/Al_2O_3(10nm)/ITO, and Au/ZnO(10nm)/Al_2O_3(2nm)/ITO—and compares them with comparable systems to justify their selection and highlight their advantages.

2.1 ZnO as switching layer

Zinc oxide (ZnO) is extensively used in RS devices due to its native oxygen-vacancy-rich structure and polycrystalline grain boundaries, which support conductive filament formation and ionic migration. A recent bilayer ZnO/Al_2O_3 RRAM demonstrated modulated multi-level resistive states by tuning current compliance, with stepwise filament disruption revealing quantized conductance behavior—ideal for analog memory and emulation of synaptic plasticity, e.g., potentiation/depression, spike-rate-dependent plasticity) [8]. Moreover, nano-crystalline ZnO memristors demonstrated reliable switching for over 200 pulses, long retention (~10^4 s), and high pattern recognition accuracy (~90%) in neural network simulations [1]. These findings confirm the relevance of ZnO as a defect-engineered switching medium with neuromorphic applicability. Also, in the work of T. Cheng et al., analog memristive devices made of Au/ZnO/ITO were fabricated by magnetron sputtering, and their results showed that the devices present analog memristive characteristics; with currents flowing through the devices in the order of μA at around 3V giving insights of the potential of ZnO-based memristors for applications in artificial intelligence [9].

Oxygen-vacancy dynamics dominate the switching physics in ZnO devices, and in some electrode configurations, metal-ion involvement also plays a role. High-resolution structural and spectroscopic studies have directly observed metal filaments and vacancy-rich conduction paths in metal/ZnO/metal stacks, confirming that conductive filaments in ZnO can be either insulating-oxide-scaffolded (oxygen-vacancy-dominated) or metal-filled, depending on the electrode chemistry and current compliance during formation. This dual nature explains why ZnO devices can exhibit significant variability in forming voltage and ON/OFF ratios across electrode choices and fabrication recipes, and also why interface engineering (for example, adding a thin Al_2O_3 barrier) can shift the dominant mechanism from stochastic bulk filamentation toward more stable, interface-modulated conduction [10].

The fabrication method critically determines the performance of ZnO based memristors. The ZnO grown by sputtering, pulsed-laser deposition (PLD), or atomic layer deposition (ALD) shows different grain sizes, density of defects, and film stoichiometry, which directly translates into the device's behavior: sputtered ZnO commonly yields polycrystalline films with abundant grain boundaries that serve as vacancy highways for CF nucleation. At the same time, ALD ZnO can provide superior thickness control and conformality for ultrathin stacks and nanometer-scale bilayers. Recent reviews on ALD films for RRAM highlight that ALD-grown oxides (including ZnO and Al_2O_3 interlayers) offer reproducible stoichiometry and thickness control, which are particularly important for enabling forming-free behavior and narrower switching distributions. Consequently, the choice of deposition technique should be considered a primary design parameter when optimizing ZnO devices for either binary memory or analog neuromorphic operation [11].

2.2 Al_2O_3 as switching layer and buffer/interfacial layer

Aluminum oxide (Al_2O_3) has become a widely used material in RS research, both as a primary switching dielectric and as an interfacial/buffer layer in bilayer and multilayer stacks. When deposited by ALD, Al_2O_3 yields highly conformal, low-defect films with excellent thickness control and stoichiometry. ALD-grown Al_2O_3 has been used successfully in trilayer stacks (e.g., $Al_2O_3/HfO_2/ Al_2O_3$) and shown to produce reliable switching, good endurance (up to 10^3), stable resistance ratio (>10) of OFF/ON states, data retention at 85°C over 10 years, and statistically narrow switching distributions when compared with less controlled deposition methods. These favorable characteristics have been demonstrated experimentally and are widely cited as a primary reason Al_2O_3 is used as a precision barrier/interlayer in modern RRAM designs [12].

As a buffer or tunnel barrier inserted between a primary oxide and an electrode, Al_2O_3 plays several distinct roles that impact device physics and metrics. First, an Al_2O_3 interlayer can act as a current-limiting tunnel barrier, reducing the effective operating current and limiting runaway filament growth, thereby lowering power dissipation and suppressing hard dielectric breakdown. Studies on ultra-thin Al_2O_3 interlayers in TiO_2 and HfO_2 systems have shown that an appropriately placed alumina layer reduces switching voltages and operating currents, while improving the thermal stability of the RESET process. Second, Al_2O_3 modifies the oxygen-vacancy landscape at the interface, acting as a controlled reservoir or kinetic barrier for oxygen ions, which alters the energetics of filament nucleation and dissolution. These two functions, current limiting and oxygen exchange control, are the primary mechanisms by which Al_2O_3 improves reproducibility and reduces variability in bilayer RRAM devices [13].

The thickness of the Al_2O_3 layer strongly determines which switching regime dominates. Thick Al_2O_3 layers (several nanometers and above) usually require higher forming SET voltages but can confine filaments and increase device robustness against permanent electrical shorts; they are therefore useful where stricter filament confinement and endurance are desired. Conversely, ultrathin Al_2O_3 (~1-3nm) often enables forming-free or low-voltage operation and promotes interface-dominated switching (Schottky/tunnel barrier modulation) rather than fully developed bulk filaments. This thickness-dependent transition (bulk filamentary ↔ interface-controlled) is reported across multiple oxide systems and is particularly relevant for neuromorphic applications where analog, gradual conductance updates and low read voltages are essential. The trade-off is that ultrathin Al_2O_3 can increase sensitivity to process non-uniformities (local thinning/pinhole formation), which may lead to early shorts or device failure if not carefully controlled [14]. Beyond pure thickness effects, engineering the Al_2O_3 layer chemistry (e.g., controlled oxygen deficiency, doping, or insertion as part of a trilayer) can tune trap densities and redox kinetics to achieve forming-free behavior and improved uniformity. For example, as presented in Sung II Park's dissertation, nitrogen doping or engineered trap distributions in alumina have been reported to produce forming-free switching by establishing a stable, uniform trap network that mediates filament nucleation in a controlled manner. Similarly, Al_2O_3, acting as an engineered interlayer between a more vacancy-rich oxide (such as ZnO, HfO2, or Ta2O5) and the electrode, has been shown to produce hybrid filaments and stabilize multi-level states. These approaches are widely used to reconcile the competing requirements of low-voltage/analog operation and long endurance [15]. Additionally, incorporating electronegative dopants into the oxide layer, such as Au, into Al2O3 has been shown to enhance switching reproducibility and support gradual SET transitions, which are desirable for analog neuromorphic applications [16].

2.3 Electrode materials: Au, Ru, and ITO

The electrode selection has a critical influence on RS mechanisms through interface chemistry and ion exchange. Gold (Au) electrodes are an important choice in memristive devices research, primarily valued for their outstanding physicochemical stability and advantageous electronic characteristics [17], [18]. As a noble metal, gold exhibits exceptional inert properties, minimizing destructive interfacial reactions (e.g., oxidation, cation intermixing) and diffusion with common switching layers such as transition metal oxides (e.g., Ta_2O_5, HfO_2, TiO_2). This significantly enhances device endurance and reduces performance variability during cycling [19], [20]. However, some studies indicate Au atoms may diffuse into ZnO, creating Zn vacancies that affect barrier behaviors [21]. Its high electrical conductivity ensures efficient charge injection at the electrode interface, while its large work function (~5.1 eV) facilitates the formation of stable Schottky barriers crucial for controlling resistive switching mechanisms, whether based on conductive filament formation or interfacial modulation [22], [23].

Gold's natural resistance to oxidation under both ambient and operational conditions helps maintain stable contact properties, which in turn improves device reliability and switching consistency [24]. These qualities make gold electrodes particularly valuable in fundamental studies that aim to isolate intrinsic switching phenomena by reducing variability induced by the electrodes themselves [25]. Despite that, challenges including high material cost, the risk of surface diffusion and filament instability at elevated temperatures, and complexities in nanoscale lithographic patterning often motivate the search for alternative or hybrid electrode materials for future scalable commercial applications [26], [27]. Nevertheless, research employing gold electrodes continues to provide essential foundational insights for uncovering the fundamental physics that govern memristive behavior.

Ruthenium (Ru) has emerged as a strategically valuable electrode—and, in some stacks, an active cation source—for resistive-switching memristors, as it combines chemical stability with uniquely controllable ion mobility. Thanks to its high work function and inert surface chemistry, Ru forms defect-tolerant, low-variability contacts to high-κ oxides, such as HfO_2 and Ta_2O_5, which sharply reduces forming voltage spread and cycle-to-cycle drift compared with conventional Pt or TiN electrodes [28]. Notably, Ru ions migrate more slowly than Ag or Cu, which enables conductive filament formation at sub-μA currents while maintaining long retention. For instance, Pt/Ta_2O_5/Ru cells, can switch reliably below 1μA and support linear, multilevel analog conductance—ideal for neuromorphic weighting [29]. Optimizing the Ru/oxide interface also helps suppress Joule heating, allowing synaptic devices to operate with pico- to femto-joule energy per event while preserving symmetric potentiation and depression slopes [30]. Beyond low-power switching, Ru electrodes can introduce intrinsic negative differential resistance, providing built-in selector functionality for high-density crossbars without the need for extra transistors [31]. Collectively, these attributes position Ru-based electrodes as a compelling route toward scalable, energy-efficient memristive memory and computing architectures.

Indium tin oxide (ITO) stands out for its transparent conductivity and smooth morphology. In several studies, ITO has functioned effectively as both a top and bottom electrode, promoting stable resistive switching, which is crucial for reliable memory and neuromorphic applications. For example, a comparative study found ZnO devices with ITO top electrodes exhibit dual volatile/nonvolatile and multistate switching—superior analog behavior compared to Ti or Ta electrodes [32]. In another study, all-optically regulated ITO/Cu_2O/WO_3/ITO memristors have demonstrated high transparency (average transmittance of 70.14%), excellent retention, and robust endurance—qualities beneficial for both electronic and optoelectronic circuitry [33]. In another case, ITO/ZnO/Al_2O_3/TaN devices exhibited synaptic behaviors, including quantized conductance, long-term potentiation, and spike-rate-dependent plasticity [8]. Furthermore, ITO can participate in interface reactions, such as forming controlled oxygen-vacancy profiles, thereby enhancing multilevel storage and conductance quantization in memristors using oxide switching layers [34]. These results support the suitability of ITO for stable synaptic emulation. ITO serves as a versatile and high-performance electrode material, advancing the development of next-generation memory and computational hardware [32], [33], [34].

2.4 Configuration-specific insights: ZnO/Al_2O_3-based memristors

Using a ZnO/Al_2O_3 bilayer or multilayered structure has proven to be a promising strategy for advancing RRAM technologies. Zinc oxide (ZnO), a wide-bandgap semiconductor, stands out for its high electron mobility and optical transparency, features that make it well-suited for integration into electronic devices. In contrast, aluminum oxide (Al_2O_3) functions as a robust insulating layer, offering strong thermal stability and a high dielectric constant. Together, these properties contribute to improved device electrical performance and operational reliability [8]. In the bilayered structure, ZnO acts as the active switching layer, while Al_2O_3 serves as a barrier or buffer layer. This configuration facilitates the formation and rupture of conductive filaments (CFs) within the ZnO layer, a mechanism central to resistive switching behavior. The presence of Al_2O_3 influences the distribution and movement of oxygen vacancies, thereby modulating the CF dynamics and improving the uniformity and stability of the switching process [35].

Recent studies have demonstrated that ZnO/Al_2O_3 bilayered memristors can exhibit both unipolar and bipolar resistive switching characteristics. The devices present a high ON/OFF resistances ratio, low operating voltages, and good endurance and retention properties. These characteristics are attributed in the literature to the regulated formation of CFs and the suppression of leakage current facilitated by the Al_2O_3 interlayer. [35]. Moreover, the bilayered structure enables multilevel resistive states, which are essential for high-density data storage and neuromorphic computing applications. The gradual modulation of conductance levels in these devices mimics the synaptic weight changes in biological systems, making them suitable for artificial synapse implementations [8]. The fabrication of ZnO/Al_2O_3 bilayered memristors typically involves techniques such as atomic layer deposition (ALD) and sputtering, which allow precise control over film thickness and composition. The resulting devices have shown promising performance metrics, including low power consumption and high switching speeds. In essence, the ZnO/Al_2O_3 bilayered architecture leverages complementary material characteristics to enhance the resistive switching performance of memristive devices. The integration of these functional layers contributes to superior device stability and switching reliability, and demonstrates strong potential for implementation in next-generation non-volatile memory and neuromorphic computing systems.

By pairing ZnO and Al_2O_3 bilayers with different bottom electrodes, this thesis evaluates how interface chemistry affects switching dynamics. The Au/ZnO/Al_2O_3/Ru stack explores the Ru's electrode role, which is underrepresented in literature and may impact the filament formation and switching variability. In contrast, Au/ZnO/Al_2O_3/ITO benefits from ITO's smooth interfaces and oxygen mobility to achieve a more analog-like, multilevel switching—consistent with reports of enhanced neuromorphic performance using ITO electrodes [32]. These device configurations, combined with variations in Al2O3 thickness (i.e., 10nm vs. 2nm), enable a systematic exploration of switching regimes, from filamentary to interface-dominated mechanisms.

In comparison to traditional TiO_2-based memristors, ZnO/Al_2O_3-based memristors can offer lower operating voltages and improved analog behavior. Other oxides, such as Ga_2O_3 or AIN/Al_2O_3 bilayers, deliver high ON/OFF ratios and retention, which are good for memory applications. For example, AIN-based memristors have improved switching by forming native Al_2O_3 during operation [36]. W/ZnO/ITO systems also showcase tunable RS behavior via bottom electrode selection [37]. Meanwhile, HfO_2/ZnO bilayer synaptic devices exhibit grain-boundary-mediated analog switching behavior that is influenced by annealing strategies [38]. The use of organic and composite systems (e.g., ZnO/PVA-MoS_2 hybrids or perovskites) further extend memory windows and fabrication flexibility, though often at the cost of CMOS compatibility and endurance [39].

2.4 Summary

In summary, ZnO/Al_2O_3 bilayered structures—especially when combined with Au, Ru, or ITO electrodes—can offer a robust platform for exploring resistive switching and neuromorphic behavior. These materials selection can enable controlled, multilevel conductance, low-voltage operation, and interface-mediated modulation. Variations in Al_2O_3 thickness and electrode materials offer leverage over switching mechanism and performance metrics.

CHAPTER 3. MATERIALS AND METHODS

The following chapter focuses on the practical aspects of the research, including the fabrication process of the memristive devices, the electrical characterization methods, and the statistical tools employed for analyzing the samples.

3.1 Fabrication of the memristive devices

The fabrication of the samples involved integrating different deposition techniques—such as atomic layer deposition (ALD) to deposit the active layer thin films, sputtering and thermal evaporation to make the electrodes—to obtain the sandwich-like MIM structures. In our structures, the devices share a common bottom electrode, as shown in Fig. 2, and each circular, patterned top electrode (deposited using a shadow mask) forms an individual device when the probe tips are connected.

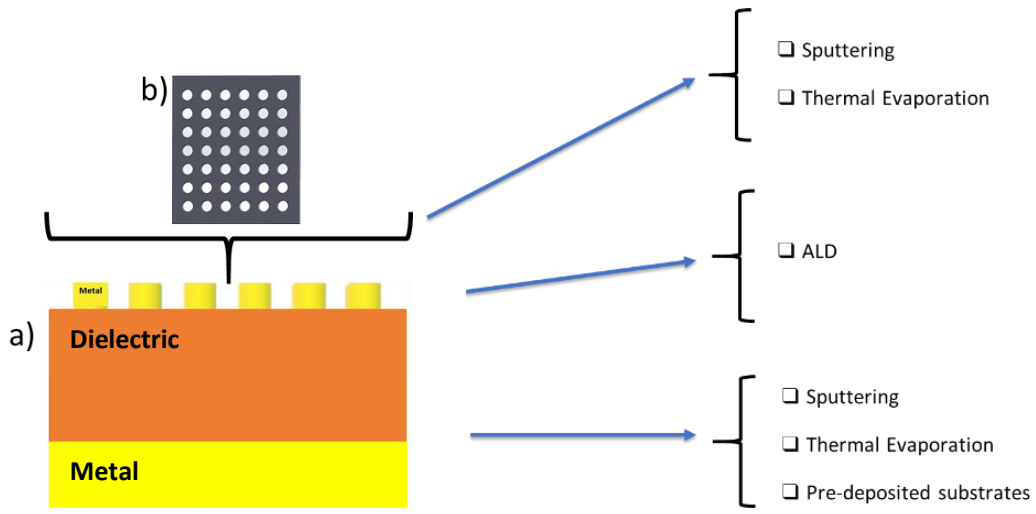

Fig. 2 | Schematics of the fabricated devices: a) typical MIM structure, b) schematic of the shadow mask with circular patterns used to deposit the top electrodes.

3.1.1 Fabrication of Au/ZnO(10nm)/Al_2O_3(10nm)/Ru memristors

For the fabrication of the Au/ZnO/Al_2O_3/Ru, we first deposited a 50nm passivation layer of Al2O3 using atomic layer deposition (ALD) on a silicon substrate. We deposited the Ru bottom electrode (BE) layer using the magnetron sputtering technique, both active layers (ZnO and Al2O3) were deposited using ALD, for the entire process the reactor temperature was set to 200°C, ZnO and Al2O3 were deposited by controlling the purge gas N2 exposure time with the controlled flow of TMA and Diethyl Zinc precursors and the oxidizer agent (H2O). To obtain the 10nm thickness of Al2O3, 100 ALD cycles were required, while the 10 nm ZnO layer was deposited with 61 ALD cycles. Then, the Au top electrodes were deposited using thermal evaporation through a 600 μm diameter shadow mask to obtain individual devices on the sample. The device's structure is presented in Fig. 3.

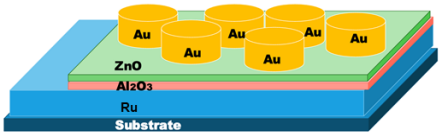

Fig. 3 | Schematics of the Au/ZnO(10nm)/Al_2O_3(10nm)/Ru structure.

3.1.2 Fabrication of Au/Al_2O_3(20nm)/ITO memristors

We utilized commercially obtained ITO-coated glass substrates (TECHINSTRO, Prod. Code TIXZ 001; 25mm x 25mm x 0.7mm; resistivity <10 Ω/sq; ITO thickness 180-200 nm). The first fabrication step involved thermally evaporating a thin Au film onto one corner of the substrate. This localized Au deposition was performed to insulate the underlying ITO bottom electrode in this area, facilitating electrical access after removing this Au patch and the overlying active layers. Following this, a 10 nm Al_2O_3 layer was deposited onto the ITO substrate by atomic layer deposition (ALD) using trimethylaluminum (TMA) and H_2O at 200°C for 200 cycles. Subsequently, individual top Au electrodes with an area of 600 μm² were patterned using thermal evaporation through a circular shadow mask. In Fig. 4, a schematic of the device structure is shown.

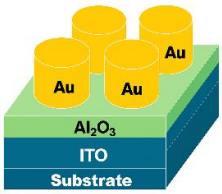

Fig. 4 | Schematics of the Au/Al_2O_3(20nm)/ITO structure.

3.1.3 Fabrication of Au/ZnO(10nm)/Al_2O_3(10nm)/ITO memristors

For the fabrication of the samples, we utilized ITO coated glass substrates as received from TECHINSTRO (Prod. Code – TIXZ 001, L25mm x W25mm x T0.7mm, Resistivity <10Ω/sq) with an ITO thickness of 180-200 nm, first we covered one corner of the substrate with a tin film of gold deposited via thermal evaporation to insulate the bottom electrode in that area from the active layer materials—this process was realized to ensure an easy access to the bottom electrode after the removal of the gold layer and the materials deposited over it—deposited by the atomic layer deposition (ALD) technique, first the 10 nm Al_2O_3 layer was deposited on top of the ITO using trimethylaluminum (TMA) as precursor and H_2O as the oxidizing agent at 200°C for 100 cycles, then the 10 nm ZnO layer was deposited using diethylzinc (DEZ) as precursor and H_2O as the oxidizing agent for 62 cycles. A circular, patterned shadow mask with an area of 600 μm² was placed over the sample to deposit the individual top Au electrodes in a thermal evaporation chamber.

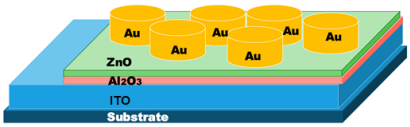

Fig. 5 | Schematics of the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO structure.

3.1.4 Fabrication of Au/ZnO(10nm)/Al_2O_3(2nm)/ITO memristors

For the fabrication of the samples, we utilized ITO coated glass substrates as received from TECHINSTRO (Prod. Code – TIXZ 001, L25mm x W25mm x T0.7mm, Resistivity <10Ω/sq) with an ITO thickness of 180-200 nm, first we covered one corner of the substrate with a tin film of gold deposited via thermal evaporation to insulate the bottom electrode in that area from the active layer materials—this process was realized to ensure an easy access to the bottom electrode after the removal of the gold layer and the materials deposited over it—deposited by the atomic layer deposition (ALD) technique, first the 10 nm Al_2O_3 layer was deposited on top of the ITO using trimethylaluminum (TMA) as precursor and H_2O as the oxidizing agent at 200°C for 100 cycles, then the 10 nm ZnO layer was deposited using diethylzinc (DEZ) as precursor and H_2O as the oxidizing agent for 62 cycles. The individual circular, patterned top Au electrodes, each with an area of 600 μm², were deposited via thermal evaporation using a shadow mask.

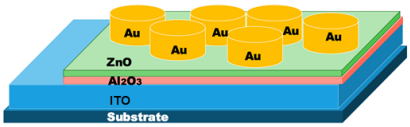

Fig. 6 | Schematics of the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure.

3.2 Electrical characterization of the memristors

To characterize the electrical response of the memristive devices, we employed a probe station configured as shown in Fig. 7, using a Keithley 2450 SourceMeter to apply ramped and pulsed voltage stresses and measure the current flowing through the devices.

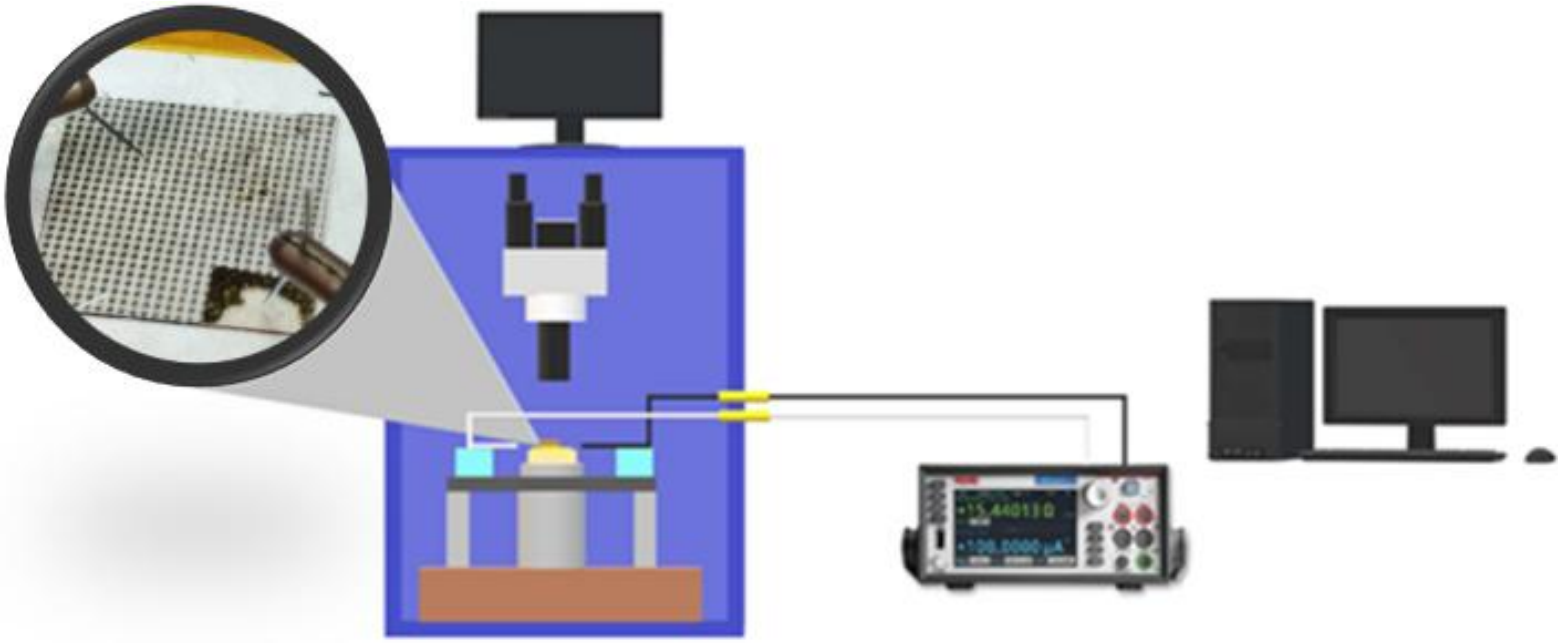

Fig. 7 | Schematics of the measurement station used to characterize the electrical properties of the samples.

3.2.1 Electroforming process

Electroforming is a crucial initial step for inducing resistive switching in most ReRAM devices, significantly defining their operational characteristics. In contrast, forming-less memristors operate without this step. For the specific device structures we fabricated, electroforming was required to achieve resistive switching: the Au/ZnO(10nm)/Al_2O_3(10nm)/Ru structure required a forming sweep from 0 to 8 V, while the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO structure required sweeps from 0 to 10 V. Conversely, devices with the structure Au/ZnO(10nm)/Al_2O_3(2nm)/ITO exhibited forming-less behavior."

3.2.2 Identifying that a memristor has been formed

Correctly interpreting the device's electrical characteristics is crucial and is highly influenced by the methods used to collect the data. Electrical tests are typically performed using a probe station setup. The most widely used figure of merit involves acquiring two current–voltage (I–V) characteristics: one corresponding to the SET transition and another to the RESET transition (Fig. 8) [40].

- Electrical tests were conducted to determine if the devices can achieve resistive switching by applying voltage sweeps within specific ranges and measuring the current to confirm the presence of hysteresis.
- Identify the threshold voltages at which SET/RESET events occur.

Even so, such proof-of-concept observations are not enough to fully explain the underlying mechanisms and performance reliability of the resistive switching (RS) behavior in metal–insulator–metal (MIM) structures. A deeper understanding requires thorough evaluation of key performance metrics— such as endurance, data retention, switching speed, power efficiency, device-to-device and cycle-to-cycle variability, scalability, and the dominant charge transport mechanisms. Moreover, it is important to note that conventional I–V sweep measurements do not accurately reflect the operational conditions of practical memory devices, which typically operate under short-duration (<100 ns) pulsed voltage stresses (PVS) [40].

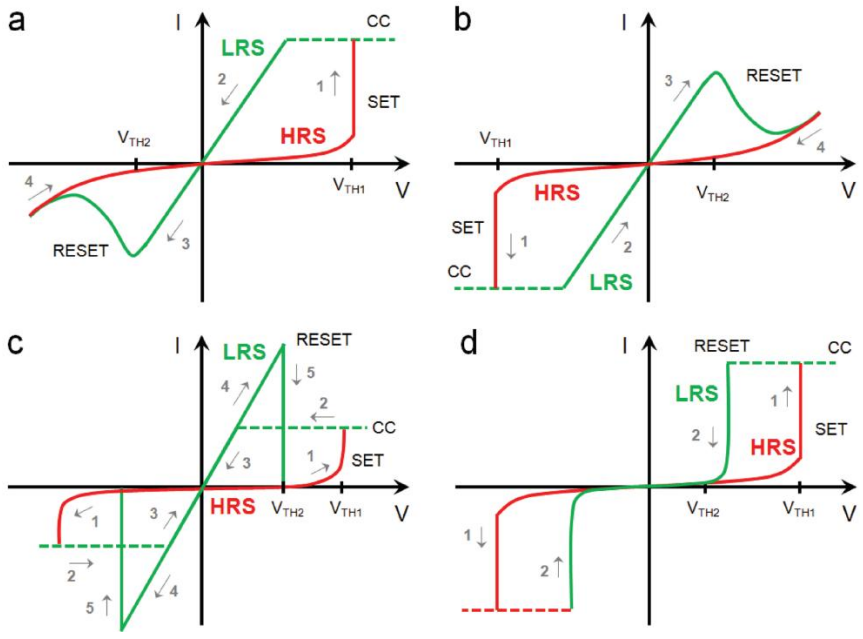

Fig. 8 | Types of resistive switching characteristics. a,b) Typical I–V sweeps showing one cycle of a bipolar RS, inducing the set with positive and negative polarities (respectively). c,d) Typical I–V sweeps showing the presence of a unipolar and threshold RS (respectively) [40]**.**

3.2.3 Evaluating the reproducibility and endurance of memristors

After confirming that the devices have achieved resistive switching, we conducted an endurance test. The device endurance is defined as the number of times it can be switched between two or more resistive states while maintaining an adequate resistance ratio [41].

- From the I-V curves, the resistive states were measured at the voltage where the largest difference between the two states was identified across all cycles.
- Pulsed voltage stresses were applied, modifying the voltages (V_{SET} and V_{RESET}) and duration times of each pulse (T_{SET} and T_{RESET}), while simultaneously measuring the current conducted. Typically, higher-amplitude pulses are employed to induce a SET/RESET in the devices, and smaller-amplitude READ pulses are inserted after each pulse to measure the device's conductance without interfering with the device state. A schematic of the PVS is presented in Fig. 9.

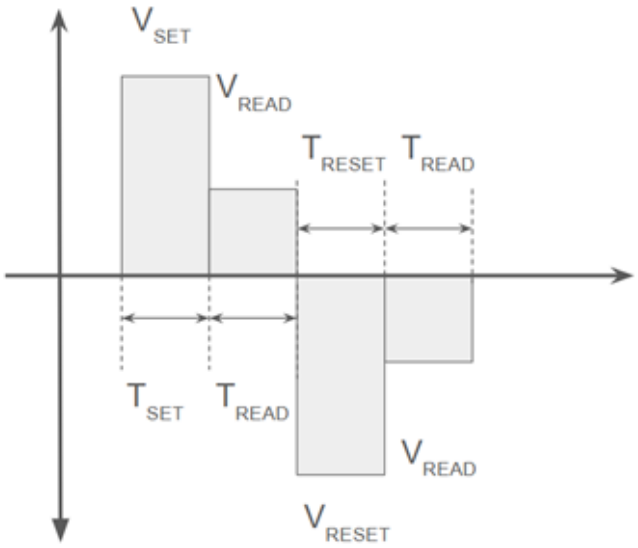

Fig. 9 | Schematics of the pulsed voltage stresses (PVS) used to evaluate the device's endurance.

3.3 Weibull analysis

Weibull analysis is a critical statistical tool that plays a key role in evaluating the reliability and failure behavior of memristors, especially in terms of endurance (cycling lifetime) and breakdown characteristics [42]. Unlike simpler statistical models, the Weibull distribution offers flexible shape control through its shape parameter (β), making it suitable to model diverse failure modes common in memristive devices. These include early-life failures (infant mortality, $\beta<1$), random failures over time (constant failure rate, $\beta\approx1$), and wear-out mechanisms that dominate later stages (aging, $\beta>1$). By fitting experimental data—such as the number of cycles to failure for multiple devices or the time/temperature to breakdown under stress—to a Weibull distribution, researchers can extract key parameters. The shape parameter (β) reveals the nature of the dominant failure mechanism, while the scale parameter (η) indicates the characteristic lifetime or stress level at which 63.2% of the devices are expected to fail [43].

This type of analysis is especially valuable because it quantifies the variability in device lifetimes, estimates failure probabilities under different operating conditions or array sizes, and helps identify weak sub-populations. Ultimately, it guides the design and fabrication of more reliable memristors with predictable performance for real-world applications like neuromorphic computing and non-volatile memory. In the following section, we outline a practical approach to performing Weibull analysis for memristive devices.

1. Define the Parameter to Analyze

Identify what parameter is going to be analyzed with the Weibull distribution:

- SET/RESET time
- Switching voltage
- Resistance at LRS/HRS
- Endurance (number of cycles before failure)

2. Collect Experimental Data

To ensure reliable Weibull fitting, gather a large dataset from experimental runs (≥ 30 data points is generally recommended for meaningful statistical analysis). For example:

- 100 SET voltages from a memristor
- Time-to-failure over repeated switching
- Resistance values after many cycles

3. Rank the Data & Calculate Weibull CDF

1. Begin sorting the dataset from smallest to largest.
2. Next, assign each data point a rank I, starting from 1 up to N, the total number of samples.
3. Then, calculate the cumulative probability for each point using the Weibull transformation.

4. Apply the Weibull Transformation

Weibull CDF is:

$$F(x) = 1 - e^{-\left(\frac{x}{\eta}\right)^{\beta}} \tag{38}$$

Taking logs twice gives:

$$\ln(-\ln(1 - F)) = \beta \ln(x) - \beta \ln(\eta) \tag{39}$$

So

- Plot ln(x) vs ln(-ln(1-F))
- A straight line suggests the data fit a Weibull distribution
- Slope = shape parameter β
- Intercept = related to scale parameter η

5. Extract Weibull Parameters

From the plot:

- Shape parameter (β): tells us the failure behavior
    - β<1: early failures
    - β=1: random failures
    - β>1: wear-out failures
- Scale parameter (η): characteristic life (value at 63.2% probability of failure)

6. Interpret for Memristors

Depending on what parameter is being analyzed:

- The Weibull spread tells us about device variability when examining switching voltages.
- When analyzing endurance, the Weibull shape indicates reliability and wear-out.

CHAPTER 4. RESULTS AND DISCUSSION

In this chapter, we present the experimental results obtained from the various devices that were fabricated and analyzed during this study. These include the Au/ZnO(10nm)/Al_2O_3(10nm)/Ru structure, the single-layer Au/Al_2O_3/ITO, the bilayer Au/ZnO(10nm)/Al_2O_3(10nm)/ITO, and finally a version with a thinner alumina layer, Au/ZnO(10nm)/Al_2O_3(2nm)/ITO. Each configuration was designed to investigate different aspects of resistive switching behavior. The performance of each device was characterized using current–voltage (I–V) measurements and endurance tests. The discussion chronologically follows the experimental workflow, focusing on analyzing key switching parameters, including SET/RESET voltages, resistance states, and overall device stability. The main goal was to link how material composition and structural modifications influence the electrical performance and to better understand how switching mechanisms can be controlled. The sequence of device designs and evaluation carried out in this thesis is summarized in Fig. 10. This flow diagram outlines the structures investigated, the challenges encountered, and the reasoning behind later design changes, all of which are discussed in this chapter.

The first set of memristors used a bilayered structure of Au/ZnO(10nm)/Al_2O_3(10nm)/Ru. The idea was that combining an active layer (ZnO) with a high bandgap oxide (Al_2O_3) could help stabilize the formation and rupture of conductive filaments. On paper, this ZnO/Al_2O_3 configuration seemed promising for achieving more uniform and stable switching. The electrode selection was made based on their physicochemical stability and Ru uniquely controllable ion mobility. Although this structure has the potential to exhibit resistive switching behavior, it lacked reproducibility between cycles in individual devices and presented high variability from device to device, rendering it unsuitable for memristive applications such as ReRAM or in-memory computing. This bad performance was attributed to different factors, such as the high rugosity of our Ru thin film (RMS Roughness = 1.349nm) or a possible competition between ZnO bulk and Al_2O_3/Ru interface for filament nucleation, which led us to replace the Ru bottom electrode with a material with less rugosity [44]. After measuring the roughness of different materials and investigating the properties of some of the widely used bottom electrodes in the literature, we decided to use commercial ITO substrates because they presented less roughness (RMS Roughness = 0.903nm) among the measured materials and also due to their unique combination of electrical conductivity and interfacial properties. ITO has been reported to function effectively as both a top and bottom electrode, promoting stable RS [45].

In view of the unstable behavior of the first structure, we needed a baseline. The bilayer introduced two variables: the ZnO switching layer and the Al_2O_3 barrier layer. To understand the cause of the problem, we first needed to isolate it and test whether Al_2O_3 alone—without the ZnO layer—could form a stable memristor using our fabrication process. By omitting ZnO, we removed factors such as its polycrystallinity, grain boundaries, and characteristic vacancy generation, which allowed us to focus solely on the interfaces between Au/Al_2O_3 and Al_2O_3/ITO and the behavior of an amorphous Al_2O_3 dielectric.

The devices based on this structure, despite suffering from electrical shorts (probably caused by pinholes in the relatively thick 20nm ALD film), still yielded useful insights. They showed that even with a smoother electrode, a single oxide layer introduces its own challenges, although resistive switching was still achievable.

Interestingly, the device-to-device performance displayed noticeable variability and even inverted polarity: the SET and RESET voltages were reversed across multiple devices within the same batch. This finding suggests that local electrode-oxide interfacial conditions, rather than overall material properties, primarily dictate the switching mode and reliability. It is also possible that some of these samples were contaminated, which could explain the inconsistent behavior and prevented us from performing a more systematic statistical analysis.

Bringing ZnO back into the structure provided the essential medium for resistive switching. In contrast to the relatively passive Al_2O_3, ZnO is a well-documented memristive oxide, recognized for its ability to easily generate and mobilize oxygen vacancies. Its non-stoichiometric nature provides a built-in reservoir of mobile ionic species that drive the formation and rupture of conductive filaments. The main idea behind this stage of the work was that a multilayered configuration could improve performance. Using the ITO platform, allowed each layer's role to emerge more clearly, without the added complication of the electrode roughness. The 10nm thick ZnO layer acted as the primary host for filament formation and rupture. Its polycrystalline nature provided grain boundaries that likely served as paths for vacancy migration and nucleation sites for filaments.

The adjacent 10nm Al_2O_3 layer functioned mainly as a barrier and current limiter. Owing to its wide bandgap and good dielectric strength, it played two important roles:

1. Interface engineering: it produced a cleaner interface with the ITO electrode, helping to confine the switching phenomenon and prevent uncontrolled oxygen exchange that may have affected the single-layer devices.
2. Filament confinement: the high bandgap Al_2O_3 helped to regulate the current flow and prevents the formation of overly thick filaments that lead to hard dielectric breakdown or irreversible changes in the devices.

The electrical measurements from the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO devices confirmed that the design worked largely as intended. The I-V curves displayed a clear bipolar behavior, showing SET transitions under positive bias on the Au electrode and RESET under negative bias—features that are typical of field-driven valence change mechanisms (VCM). Although this configuration marked a clear step forward, the results also revealed some remaining issues. In particular there was a large cycle-to-cycle variability in the HRS with a coefficient of variation of about 82%, and the devices still required a relatively high electroforming voltage of around 8V. These effects can be directly attributed to the large size of the top electrode (600 µm in diameter). At this macro-scale, several conductive filaments can form and rupture in simultaneously across the vast electrode area. The stochasticity of which filament dominates in any given cycle leads to the observed HRS variability. The high electroforming voltage is required to initiate the filament formation through the 20nm stack.

The development of the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO device marked the final stage of this work. This configuration combines the advantages of ZnO—its vacancy-rich, polycrystalline nature—with the interfacial control provided by an ultrathin Al_2O_3 barrier, while also taking advantage of the smoother surface and stable electrochemical behavior of the ITO electrode. Reducing the thickness of the Al_2O_3 layer from 10nm to 2nm was intended to lower the electroforming voltages, promote more uniform filament formation, and minimize the stochasticity associated with incomplete filament rupture.

Even so, the thinner barrier introduced a different set of challenges. Although the endurance of the devices improved substantially compared with earlier designs, they still tended to fail after a few hundred cycles. This degradation is primarily attributed to possible interfacial oxidation, pinhole formation in the ultrathin Al_2O_3, and progressive dielectric breakdown under repeated switching. Furthermore, the ON/OFF ratios, although sufficient for binary operation, still falls short of the values reported in state-of-the-art multilayered memristors. These findings emphasize the inherent trade-offs in ultrathin-barrier design: while thinning enhances forming-free operation and lowers variability, it also increases sensitivity to local defects and accelerates wear-out mechanisms.

The steady progression—from the initial Ru-based bilayers to the single-layer Al_2O_3 on ITO, then to the ZnO/Al_2O_3 bilayers, and finally to the optimized 2nm Al_2O_3 design—reflects the iterative approach taken throughout this work. Each configuration, despite its challenges, provided important insights into how electrode morphology, oxide selection, and layer thickness influence resistive switching performance. Overall, the findings discussed in this chapter highlight how careful material and structural engineering can tune memristor performance, moving from unstable, highly variable switching toward more consistent and controllable device operation. This gradual improvement suggests promising directions for future ReRAM and neuromorphic applications.

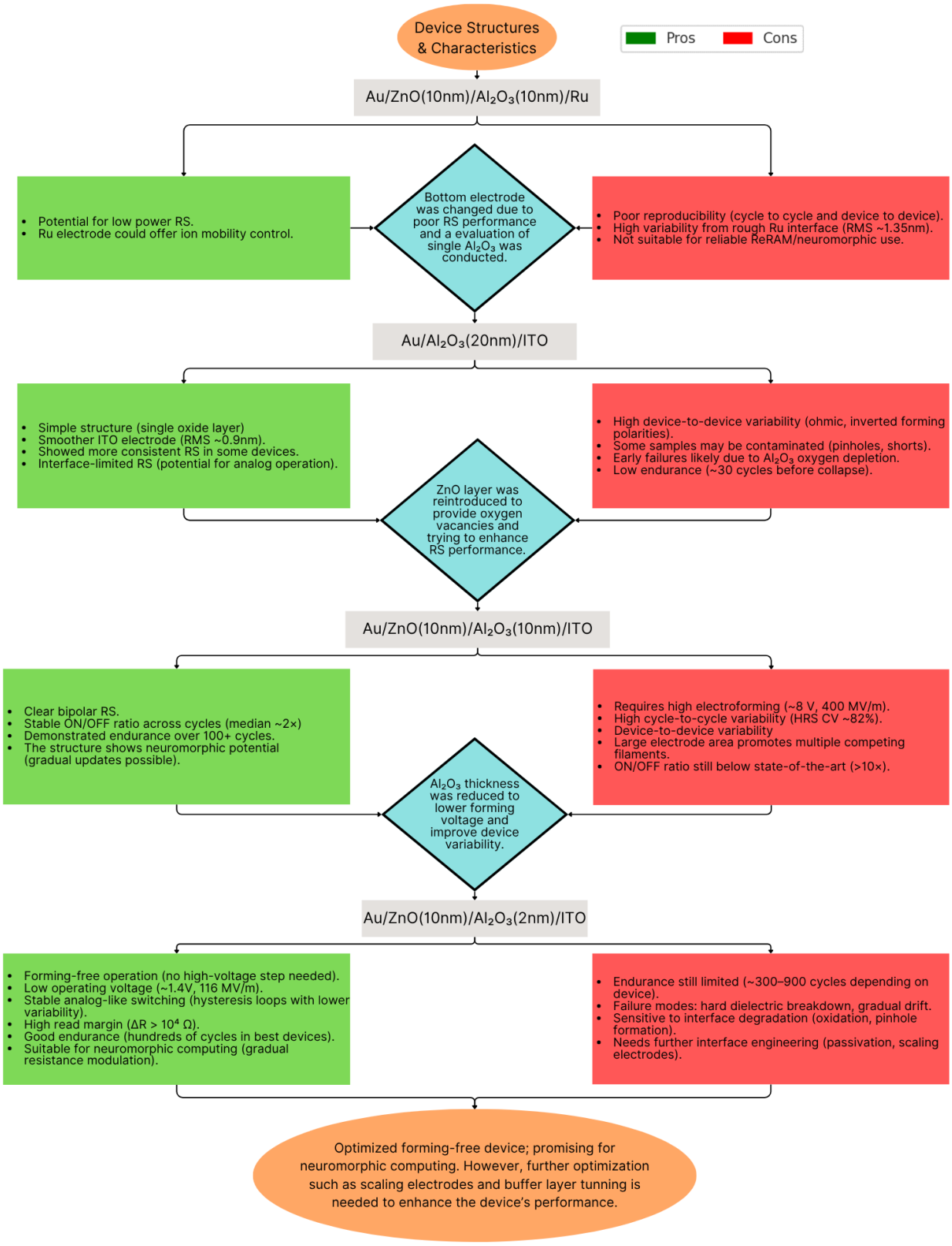

Fig. 10 | Flow chart of the device's structures and characteristics.

4.1 Au/ZnO(10nm)/Al_2O_3(10nm)/Ru structure findings.

The first structures we designed were stacks of bilayer ZnO(10nm)/Al_2O_3(10nm) sandwiched between Au (top electrode) and Ru (bottom electrode) as shown in Fig. 3; this specific materials selection was based on the literature evidence of the potential to achieve resistive switching on ZnO thin films [1], [8], [46], [47] and the barrier properties of Al_2O_3 layer which on paper should help controlling the distribution and movement of oxygen vacancies, thereby modulating the CF dynamics and improving the uniformity and stability of the switching process [8], [35]. However, this device's structure did not perform well enough to obtain reproducible I-V hysteresis in cycle-to-cycle or device-to-device voltage sweeps. The pristine state of the devices was measured with chronoamperometry, which exhibited a charge and discharge curve characteristic of the capacitors with a capacitance of 0.988 nF. It can also be seen that the devices have potential for its use as a battery since it does not discharge completely as shown in Fig. 11, the electroforming was performed by applying voltage sweeps from 0 to 8V at a compliance current of 100 nA to prevent irreversible changes in the material such as dielectric breakdown (in Fig. 12 is presented an example of the electroforming process of three randomly selected devices in a sample).

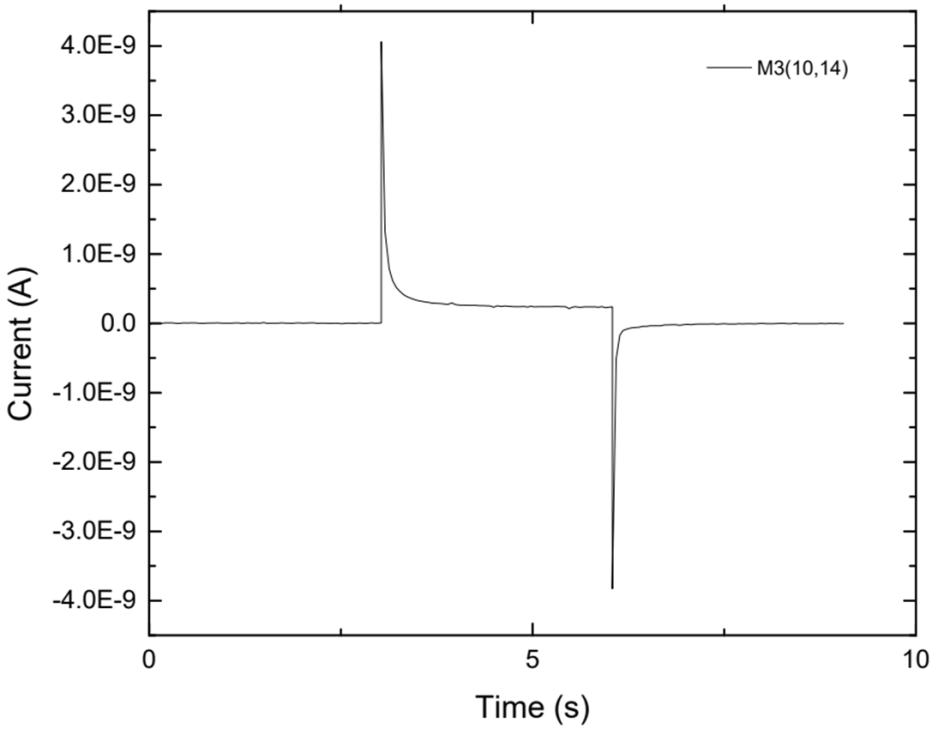

Fig. 11 | Charge and discharge plot obtained from chronoamperometry applied before electroforming to evaluate the pristine state of the structure, showed a capacitive behavior with a capacitance of 0.988 nF at 1V.

The electroforming process of three randomly selected devices, as shown in Fig. 12, illustrates the inherent stochasticity in filamentary resistive switching devices; it can be observed that the forming voltages vary from device to device. The significant variation in forming voltage results from local nanoscale variations in material properties and defect distributions beneath the large Au top electrode, particularly within the ZnO/Al_2O_3 bilayer stack. The device D3 apparently encountered a "weak spot" with high defect density or ZnO's oxygen vacancies that enabled filament formation at a lower voltage, while the device D4 required a higher voltage to overcome a more robust region.

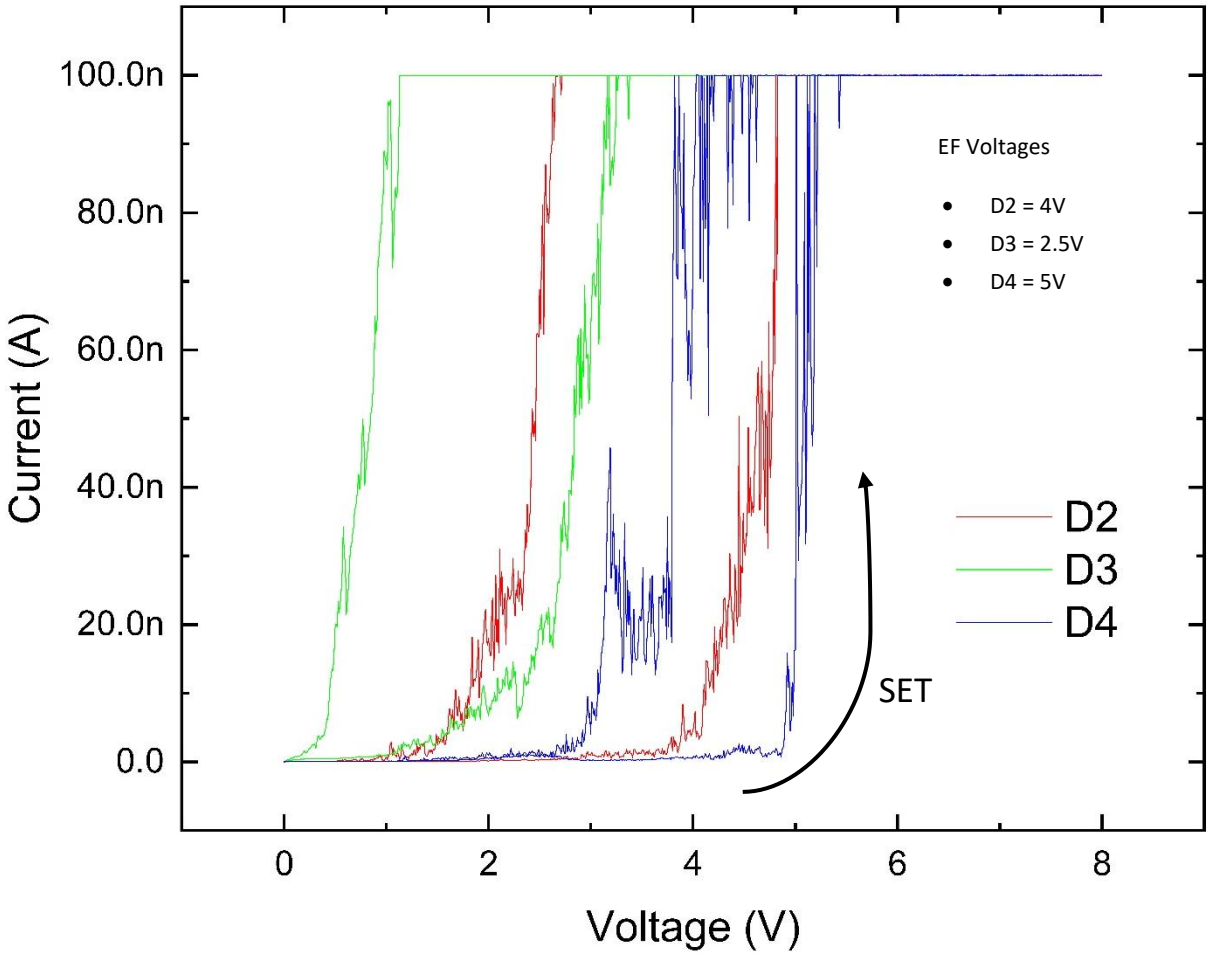

Fig. 12 | Electroforming process of three randomly selected devices in a sample of Au/ZnO(10nm)/Al2O3(10nm)/Ru. It can be seen that there is variability between the forming voltages of each device: D2 = 4V, D3 = 2.5V, D4 = 5V.

Additionally, it is worth noting that the lower forming voltages in devices D2 and D3 correlate with their higher post-forming conductance, suggesting the filament formed in these devices is likely thicker, more conductive or better connected (e.g., formed along a path rich in favorable defects/vacancies). Conversely, the higher forming voltage of device D4 and lower post-forming current suggest a thinner, less perfect, or more constricted filament path. All devices show a sharp current jump, confirming the formation of a CF. Another major contributor to the poor reproducibility and widespread forming voltages observed in the devices could be the roughness of the Ru bottom electrode, which introduces intrinsic randomness through localized electric field enhancement, dielectric thickness variation, and potentially altered interfacial reactions at nanoscale asperities. The large top electrode samples this random roughness landscape, resulting in significant device-to-device differences, as shown in Fig. 12.

We observed that this structure also lacked to achieve reproducibility in the cycle to cycle I-V electrical response after applying voltage sweeps to different devices; the Fig.13a shows the behavior of one randomly selected device in one of the samples, the stack exhibits intrinsic instability, randomly switching between non-volatile filamentary RS (in the second quadrant of the plot) and volatile interface-controlled threshold switching (TS). This instability is likely given by:

- Competition between ZnO bulk and Al_2O_3/Ru interface for filament nucleation [44].
- Ru-induced oxygen scavenging creates interfacial V_o reservoirs [44].
- Ru roughness amplifying stochasticity [48].

Such extreme cycle-to-cycle variability makes this device unreliable for conventional memory applications (e.g., ReRAM). The random occurrence of volatile cycles prevents consistent non-volatile state programming. However, if controllability can be improved, the coexistence of volatile and non-volatile switching might be exploitable in neuromorphic computing (e.g., emulating short-term/long-term plasticity) [49], [50]. This data reveals a complex and unstable interplay between filamentary and interfacial switching mechanisms in the ZnO/Al2O3 bilayer, heavily influenced by the properties of the Ru bottom electrode. This high cycle-to-cycle variability clearly shows how difficult it is to achieve reliable operation with this particular device structure.

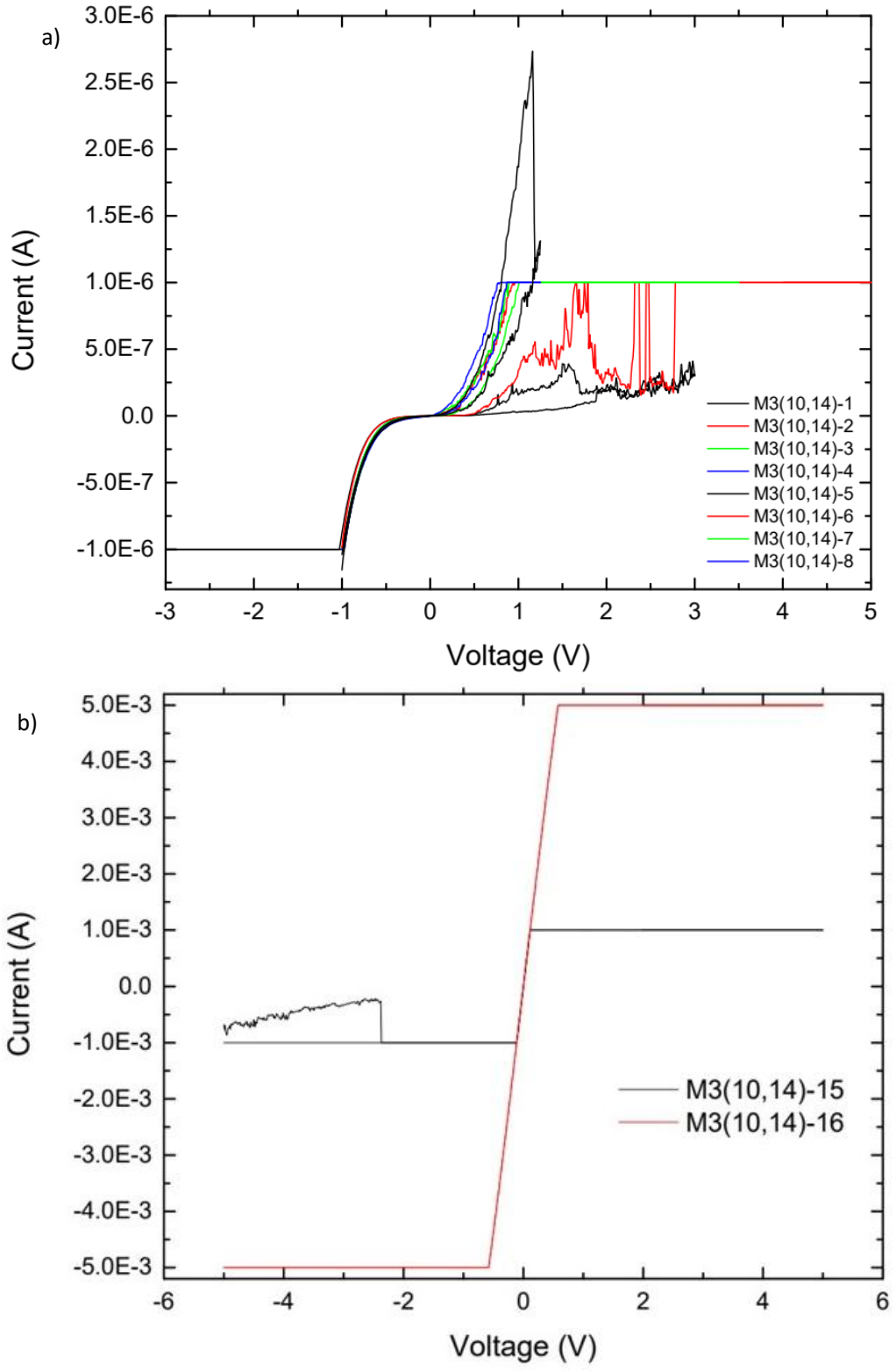

Fig. 13 | I-V curves obtained from a randomly selected device in a sample of Au/ZnO(10nm)/Al2O3(10nm)/Ru, a) first 8 cycles obtained after applying different sets of voltage sweeps. b) last two cycles after the device suffered irreversible changes that led to an ohmic contact.

The pronounced device-to-device variability observed in the Au/ZnO(10nm)/Al2O3(10nm)/Ru memristors highlights the strong influence of interfacial heterogeneity on switching behavior. Figure 14 shows the I-V characteristics for five representative devices, and Table 1 summarizes their main parameters. From these measurements, it seems that the morphology of the Ru interface largely determines the stability of the switching process [44]. Device D1 displayed clear bipolar switching (SET +2.5V/RESET -3.0V, ON/OFF=10^3), whereas the device D2 exhibited polarity inversion (SET -4.0V). Crucially, D4 demonstrates functional but marginal bipolar switching (SET: -3.5V/RESET: +3.5V) with a low ON/OFF ratio (about 3×), suggesting incomplete filament rupture due to Ru-anchoring effects. D3 remains irreversibly formed (SET +4.5V, no RESET), and device D5 showed a short-circuit response. Taken together, this hierarchy of performance—from robust to marginal functionality—directly correlates with nanoscale variations in Ru's interfacial properties: smooth regions enable stable switching (D1), moderate roughness causes weak filament control (D4), and extreme asperities trigger polarity inversion (D2) or shorts (D5). The results establish that Ru electrode engineering must achieve atomic-scale interfacial control to ensure reproducible memristive operation.

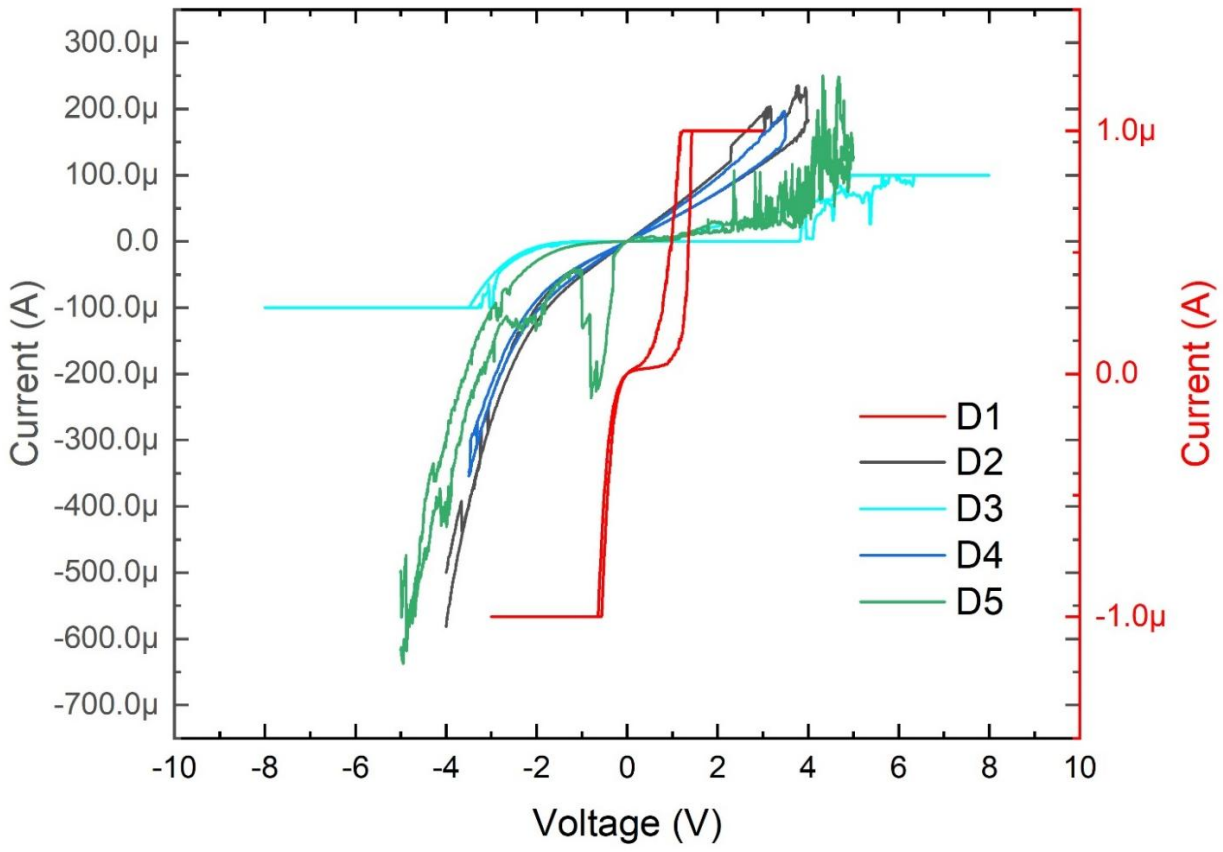

Fig. 14 | I-V curves obtained from five randomly selected devices in a sample of Au/ZnO(10nm)/Al2O3(10nm)/Ru.

Device	Switching Type	SET Voltage	RESET Voltage	ON/OFF Ratio	Status
D1	Robust Bipolar RS	+2.5 V	-3.0 V	1000	Functional
D2	Inverted Polarity RS	-4.0 V	+2.0 V	100	Functional
D3	Unstable Filamentary RS	+4.5 V	None	<2	Defective
D4	Bipolar RS (Weak)	-3.5 V	+3.5 V	3	Marginal ON/OFF ratio
D5	Parametric Short	N/A	N/A	< 2	Failed

Table 1 | Switching characteristics obtained from five randomly selected devices in a sample of Au/ZnO(10nm)/Al2O3(10nm)/Ru.

4.2 Au/Al_2O_3(20nm)/ITO structure findings.

Looking for better reproducibility devices with the structure of Au/Al_2O_3(20nm)/ITO were fabricated to analyze its electrical response; we decided to replace the Ru bottom electrode with ITO due to their rugosity differences (our Ru thin films presented an RMS Roughness of 1.349nm after ALD while the RMS Roughness for the ITO substrates was 0.903nm measured by AFM), the pristine state of these devices was variable, some of the randomly selected devices from the samples showed charge and discharge curves characteristic of capacitors after applying chronoamperometry. However, the majority of the devices had an ohmic response as a resistor with some devices conducting more than others; such behavior could indicate that the devices where in short due to possible contamination in the fabrication process that made the Al_2O_3 layer more porous in different areas of the thin film (i.e., the Al_2O_3 layer didn't deposited uniformly) causing the gold from the top electrode to seep through the pores in the thermal evaporation process making direct contact with the lower electrode as can be seen in Fig. 15 that the variation in the currents represents that in some devices as D1 a better contact with the top and bottom electrode occurred (due to the possibility of a greater density of pores or bigger pores causing more gold to make contact with the ITO BE) resulting in less resistance.

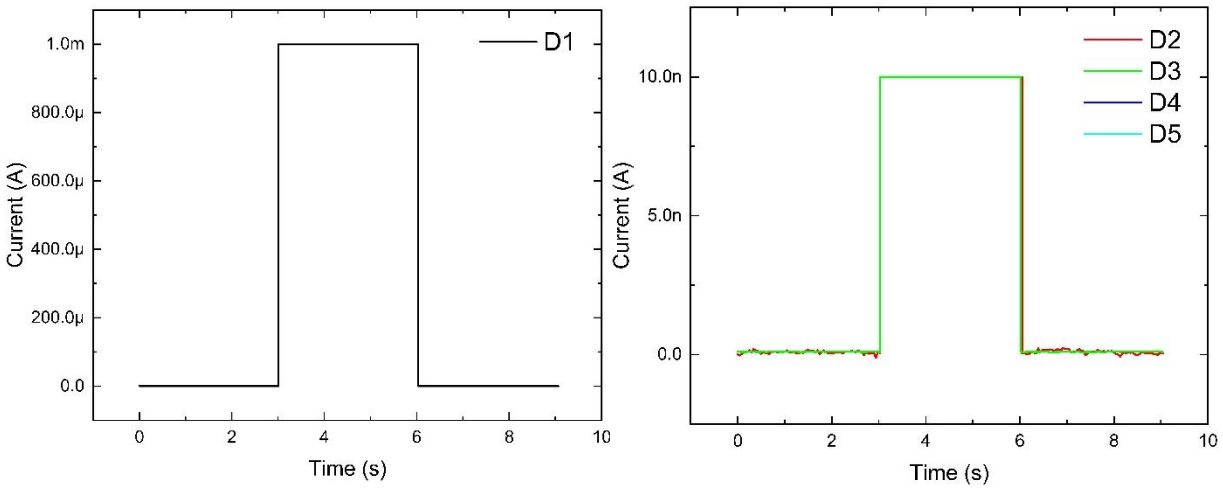

Fig. 15 | Pristine states of different Au/ZnO(10nm)/Al2O3(10nm)/Ru devices.

The majority of the Au/Al_2O_3/ITO devices are electrically short-circuited in the pristine state. After the electroforming, the devices exhibited a bipolar, filamentary resistive switching with little but notable cycle-to-cycle variability showed in Fig. 16. While this variability poses challenges for digital memory applications, it may be exploitable for neuromorphic computing where achieving multiple conductive states mimics a biological synapse [49], [50]. Further studies on pulse-mode switching and temperature effects could provide deeper insights into the switching mechanism. The I-V curves in Fig. 17 show clear hysteresis loops, indicating resistive switching between HRS and LRS. The switching is bipolar, with the SET process occurring at positive voltages and the RESET at negative voltages. The memristor device exhibited a complex, non-linear lifecycle characterized by three different phases: an initial period of switching stabilization (cycles 1-4) with moderate hysteresis (~22% more with respect to the first cycle), followed by progressive degradation through filament overgrowth and top electrode oxidation (cycles 5-7) that collapsed hysteresis (<1% with respect to the first cycle) and increased conductivity by 47% more than in the first cycle indicating ohmic conduction at positive voltages, culminating in an unexpected rebirth in cycle 10 where the resistive switching spontaneously recovered.

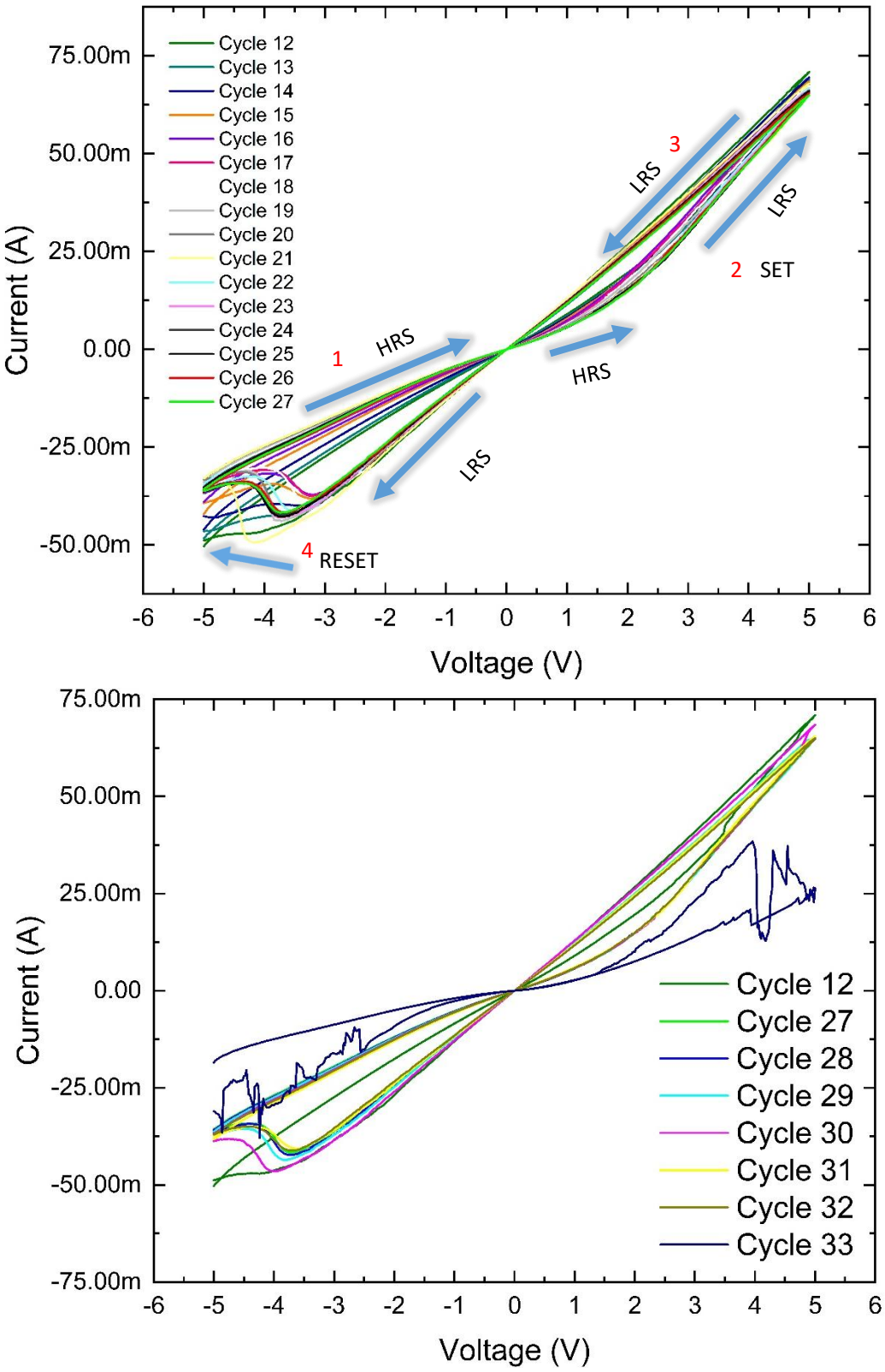

Fig. 16 | I-V curves obtained from a randomly selected device in a sample of Au/Al2O3(20nm)/ITO.

The behavior of the 10 initial cycles suggested that the device experimented a significant electroforming and stabilization phase, featuring prominent hysteresis loops with symmetric SET/RESET transitions at ±4V, but suffers from cycle-to-cycle resistance variability exceeding a 30% CV. Positive voltage sweeps showed a diminished resistance ratio (HRS/LRS decreasing to 1.11), perhaps due to Schottky-limited injection at the Au/Al2O3 interface. Negative voltage operations, however, exhibited enhanced switching contrast (ratio increasing to 1.32), likely due to cathode-optimized filament rupture at the ITO interface. Crucially, after cycle 18, the device achieves remarkable stabilization with less than 5% cycle-to-cycle variation in hysteresis characteristics. This stabilized phase exhibits consistent asymmetric switching dynamics, characterized by gradual SET transitions during positive sweeps (3-5V) and abrupt RESET events at -3.8V to -4.3V during negative sweeps, maintaining reproducible resistance states (LRS = 98-102Ω, HRS = 130-135Ω) throughout cycle 32.

The progression from a volatile forming to consistent operation suggested interface-limited switching mechanisms where ITO electrode oxidation ultimately creates preferential vacancy mobility pathways, which enabled a stable memristive behavior suitable for a crossbar array integration. However, cumulative oxygen loss permanently depleted vacancy sources by Cycle 33, collapsing the hysteresis through a possible irreversible over-oxidation. This progression illustrates how electrode-dependent electrochemical kinetics influence the stabilization and eventual failure of metal oxide memristors. The low endurance of the device could be heavily influenced by material degradation due to high currents (tenths of mA) flowing through the device that can trigger different degradation mechanisms—such as Joule heating, in which local temperatures that can reach >500°C melt/disrupt filaments (stochastic switching failure); Electromigration, where metal ions (Au/In) oversaturate the filament (hard electrical shorts); Oxide damage, occurring due to irreversible breakdown caused by high E-field (pinhole growth in Al_2O_3); and Interfacial Reactions occurring at Au/Al_2O_3 or Al_2O_3/ITO interlayers forming parasitic resistance changes—at 50mA and ~100 Ω (LRS), power dissipation equals 0.25 W which for the typical area of the devices fabricated causse massive local heating.

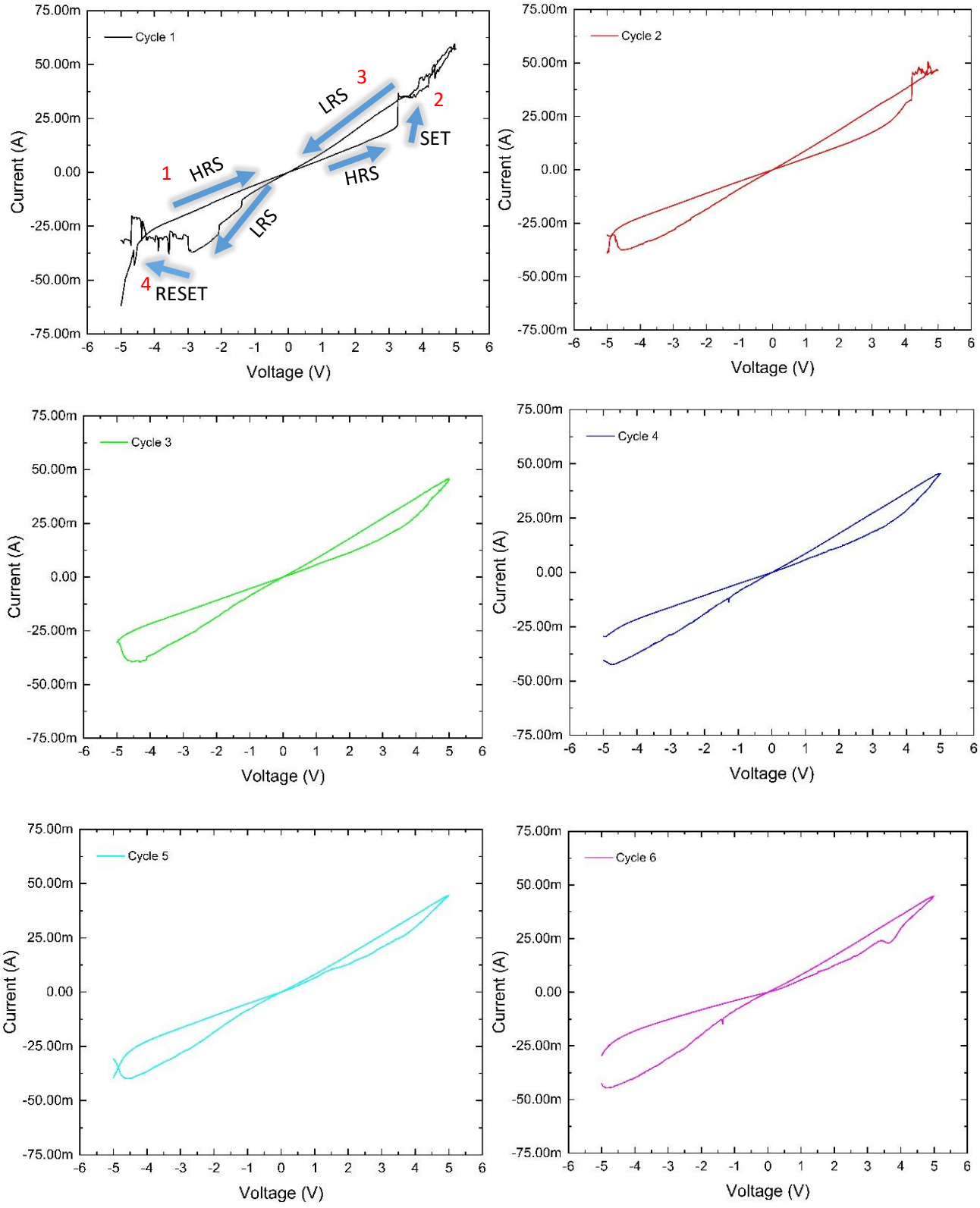

Fig. 17 | I-V curves of cycles 1-6 from a randomly selected device in a sample of Au/Al_2O_3(20nm)/ITO.

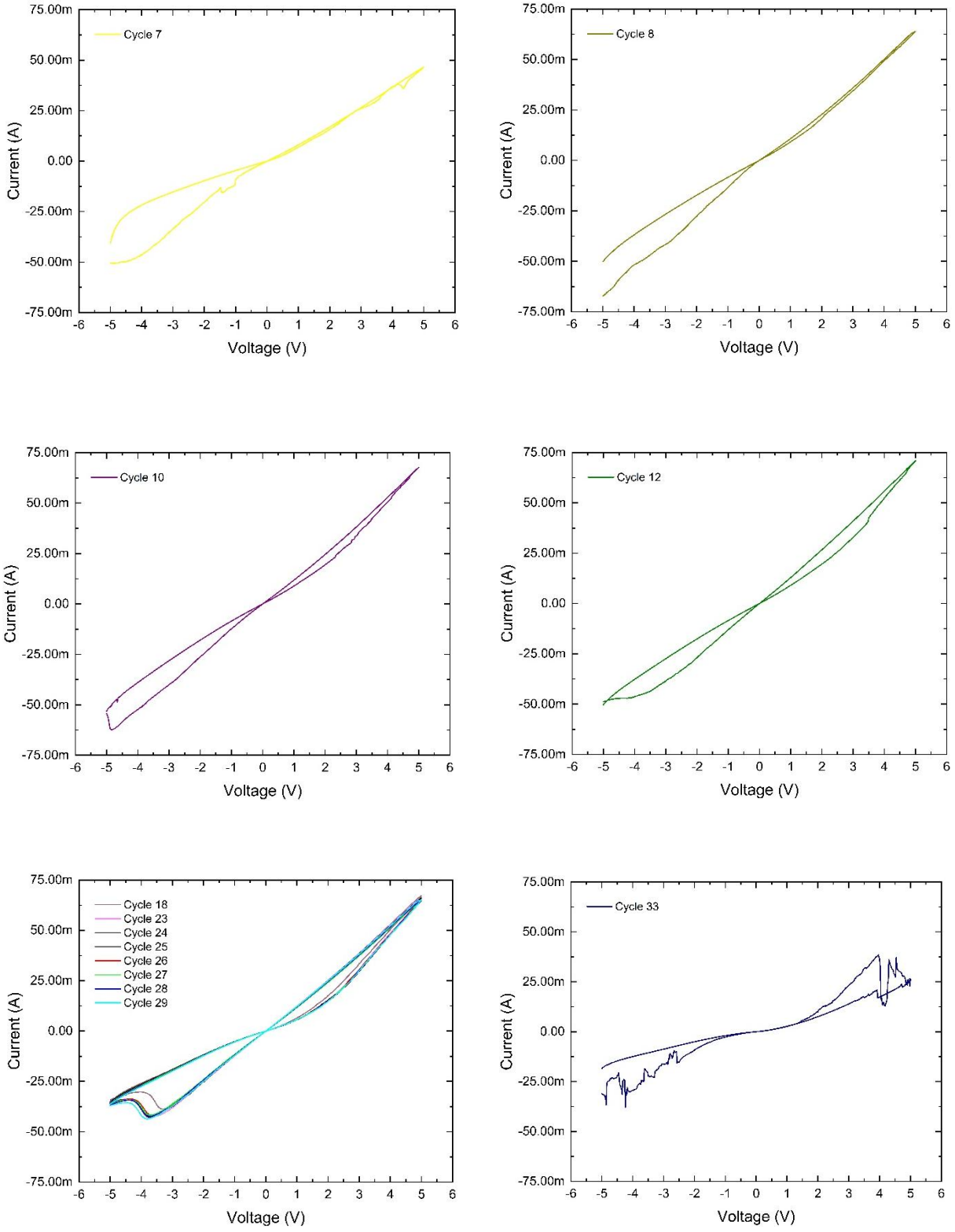

Fig. 18 | I-V curves of cycles 1-6 from a randomly selected device in a sample of Au/Al_2O_3(20nm)/ITO.

The device-to-device characteristics of the same sample of this structure showed variability. The fabricated Au/Al_2O_3/ITO memristors presented three different operational modes showed in the figure 19: (1) permanently stuck ohmic devices like a resistor that showed no hysteresis as the device “D3”, (2) conventional switching with SET transitions at positive voltages and RESET at negative voltages as the device “D7” (which failed at cycle 33 from possible Al_2O_3 oxygen depletion due to the high currents), and (3) inverted-polarity devices where SET/RESET voltages were reversed as in the device “D3”. This behavior—observed across multiple devices—stems from stochastic interfacial properties at the electrode/oxide junctions, where local variations in Schottky barriers and oxygen vacancy gradients govern the switching polarity and eventual failure mechanisms. Conventional and inverted switching polarities within the same wafer demonstrate how local electrode/oxide interfacial properties—not global material characteristics—govern operational mode and reliability in memristive devices [12], [13], [14], [15]. However, the possibility of contamination in these samples renders them unsuitable for a more thorough statistical analysis, due to the difficulty of accurately correlating the physical structure with the electrical response.

Variability Type	Root Cause	Experimental Signature
Stuck Ohmic	Metal filament penetration	Ohmic conduction
Inverted Polarity	Local Al_2O_3/ITO interface degradation	Negative SET threshold voltage
Early Failure	Al_2O_3 stoichiometry drift	

Table 2 | Possible physical origins of variability in Au/Al_2O_3(10nm)/ITO devices.

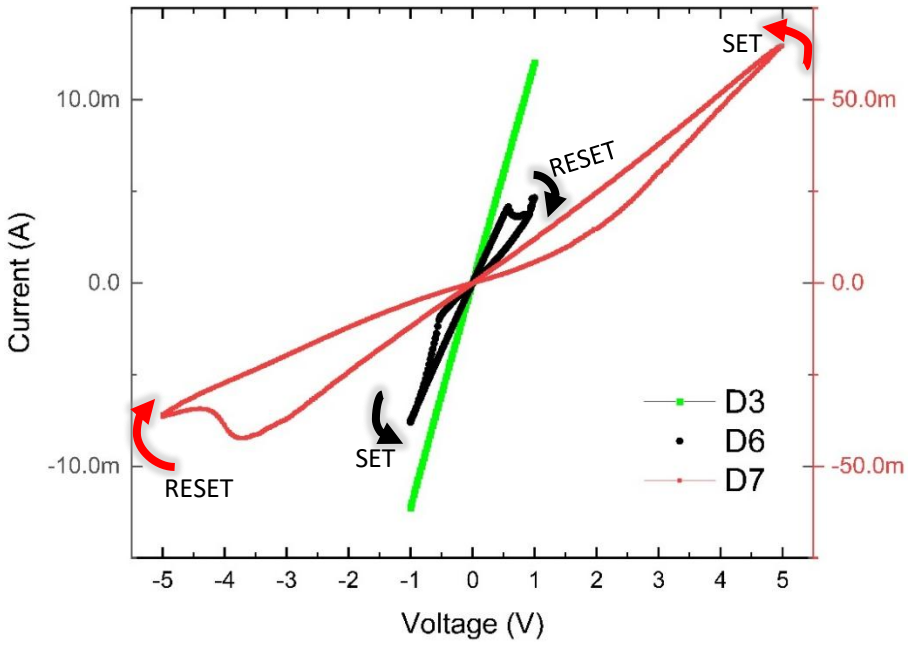

Fig. 19 | I-V curves collected from randomly selected devices in a sample of Au/Al_2O_3(20nm)/ITO showing the primary operational modes.

4.3 Au/ZnO(10nm)/Al_2O_3(10nm)/ITO structure findings.

Given the results obtained with the previous structures, it was decided to fabricate devices with the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO configuration and their electrical response was analyzed. The electroforming process in these devices was explored by applying different voltage sweeps from 0 to 10V and 0 to -8V with voltage steps of 20mV and a current compliance of 5mA, in the Fig. 20 can be observed the most representative electrical responses of the electroforming processes applied, under positive voltages (Fig. 20b) the electroforming showed an abrupt change in current indicating a filamentary type of switching via vacancy migration in ZnO while under negative voltages (Fig. 20a) a gradual change in the current was observed indicating an interfacial type of switching dominated by Schottky barriers; the devices started switching to LRS at around 8V (which means that the filament formation required an average electric field of 400 MV/m across the 20nm bilayer) for positive voltages while the devices electroformed with negative voltages started to gradually switch at about -5V (250MV/m) and fully transitioned to LRS at -7V (350 MV/m). This polarity asymmetry shows the bilayer's role modulating the switching mechanisms.

The cycle-to-cycle variability of one representative device of this bilayer structure is presented in Fig. 21. The distinct HRS and LRS in the linear scale I-V plots (Fig. 21a) clearly showed a stable bipolar resistive switching behavior. The current changes significantly at specific positive and negative voltages (SET and RESET processes), confirming the device's memristive behavior.

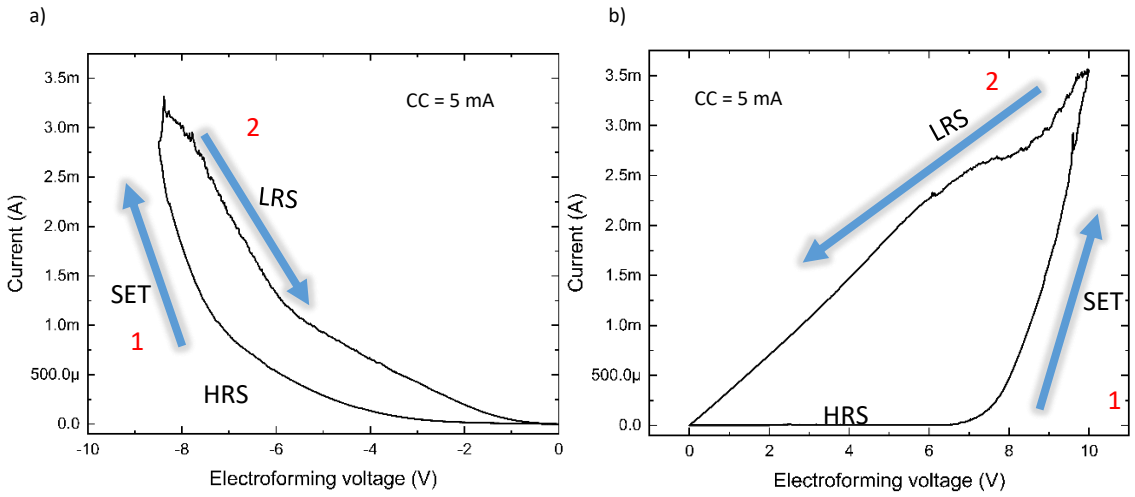

Fig. 20 | Electroforming process of the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO structure, a) electroforming with negative bias, b) electroforming with positive bias.

The obtained results showed that the device maintained reversible switching without failures. The logarithmic scale I-V plotted over 107 cycles (Fig. 21b) demonstrated robust endurance but revealed significant cycle-to-cycle variability; abrupt SET/RESET transitions were observed, suggesting oxygen-vacancy-mediated conductive filament formation and rupture in the ZnO/Al_2O_3 bilayer. The cycle-vs-resistance plot presented in Fig. 21c shows the HRS instability and LRS consistency. It can be seen that the resistance fluctuates markedly in the high resistance regime, likely due to incomplete filament dissolution or interfacial charge trapping. At the same time, the tight clustering of LRS values confirms the reliability of filament reconstruction. The variability of the resistive states can be confirmed by the calculated coefficient of variation (CV), which is 43.8% for the LRS and 82.3% for the HRS, as presented in Table 3. The HRS inhomogeneous filament rupture due to possible thermal gradient variations during RESET or oxygen vacancy clustering at ZnO grain boundaries. The LRS drift could be attributed to progressive material oxidation resulting from residual oxygen migration or ambient conditions.

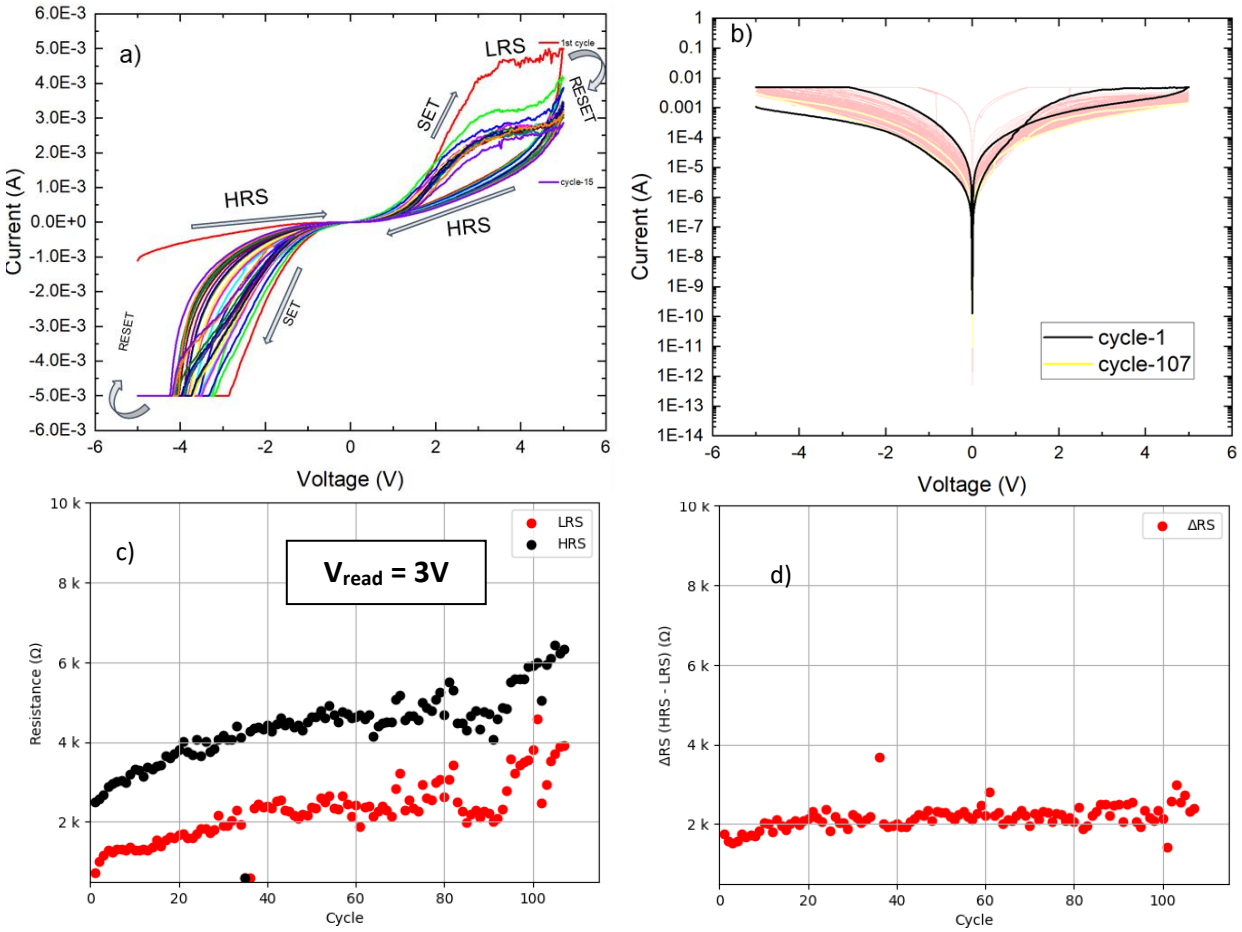

Fig. 21| Cycle to cycle variability from a randomly selected device in a sample of Au/ZnO(10nm)/Al_2O_3(10nm)/ITO structure after electroforming, a) linear I-V plots identifying the resistive states, b) log10 I-V plots of 107 cycles, c) cycle vs resistance plot showing the variability of the device, d) the difference between resistive states ΔRS (HRS – LRS) remains stable trough the cycles indicating consistent memory window.

State	Range (Ω)	Trend	Variability (CV)
LRS	600–4,582	Gradual upward drift	43.8%
HRS	2,487–6,434	Increasing dispersion with cycling	82.3%

Table 3 | Cycle-to-cycle variability.

The ΔRS plot is presented in Fig. 21d and can be observed that the device maintains remarkable stability with median 2,093Ω and interquartile range (IQR) 1,216Ω across 107 cycles, confirming consistent resistive window preservation despite significant HRS fluctuations (HRS CV=82.3% vs ΔRS CV=49.6%); for memory applications, ΔRS stability compensates for HRS variability, though interface engineering is needed to improve HRS/LRS ratio, also a stable difference between the resistive states ensures reliable read margin for binary storage. The memristor exhibits good stability in its ON/OFF ratio (HRS/LRS) across 107 cycles (Fig. 22), maintaining a median value of 2.00 with an IQR of 1.85-2.25kΩ. This consistent behavior—where 92% of cycles delivered a ratio >1.5—is particularly notable given the significant individual HRS fluctuations (CV=82.3%), suggesting that the ZnO/Al_2O_3 bilayer actively stabilizes the resistive window through complementary functions: ZnO supplies oxygen vacancies for reliable LRS formation [51], while Al_2O_3 confines the filament dissolution process during RESET to prevent HRS runaway [8], [52].

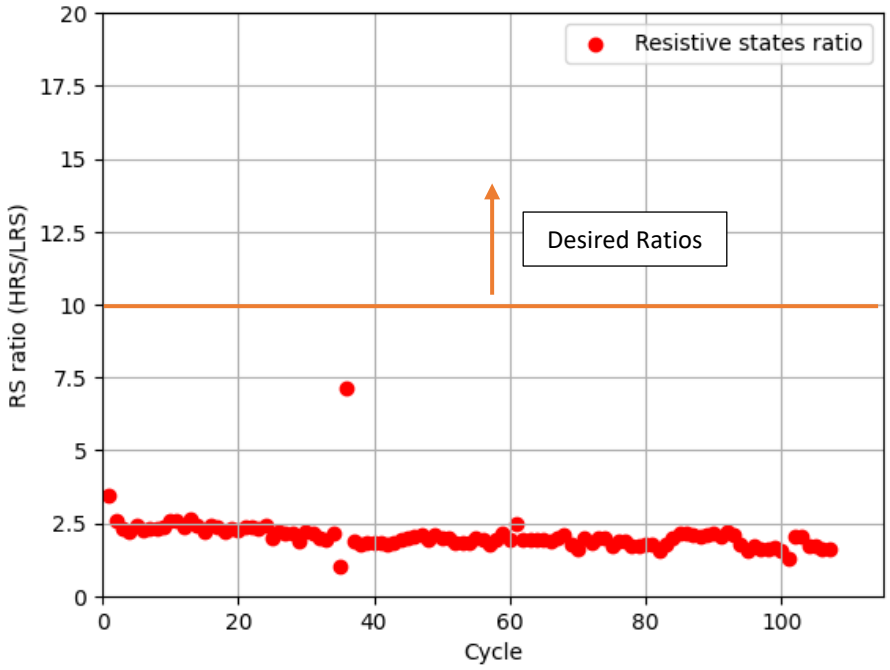

Fig. 22 | Cycle-to-cycle ON/OFF ratio

Transient anomalies—such as the unity ratio at cycle 35 (temporary dielectric breakdown) and the peak ratio of 7.14 at cycle 36 (over-reset-state)—demonstrated self-recovery without progressive degradation. Though the moderate median ratio of about 2x falls below the values reported for state-of-the-art memristors in the literature that typically are above 10x [1], [8], [53], the 30.8% coefficient of variation outperforms single-oxide memristors that present values of the 40-70%, ensuring sufficient read margin for binary memory applications. The late-cycle ratio decline observed after the cycle 100 suggests that interfacial oxidation is the primary endurance limiter, highlighting a target for future interface engineering to enhance the memory window without compromising the device endurance.

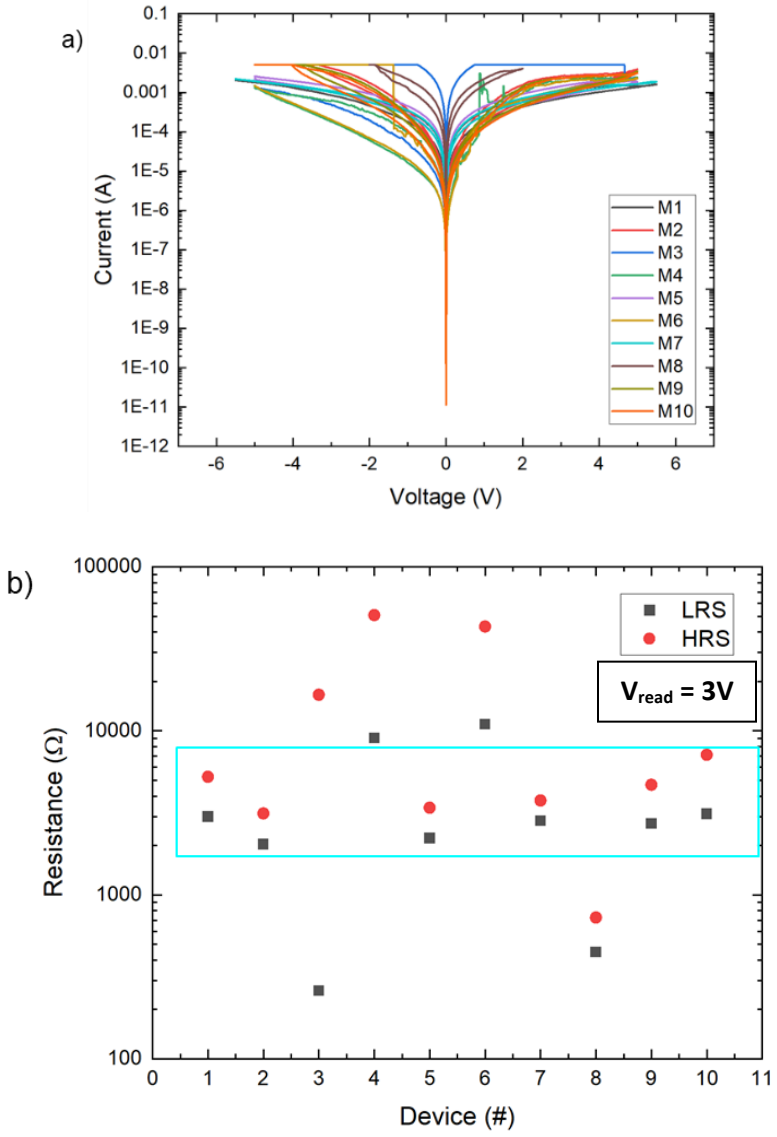

Fig. 23 | Device-to-device reproducibility, a) I-V curves collected from 10 randomly selected devices of ZnO(10nm)/Al_2O_3(10nm)/ITO, b) Device vs resistance plots of the 10 devices measured at -0.5V showing the reproducibility of the devices.

The Au/ZnO(10nm)/Al_2O_3(10nm)/ITO memristors exhibit extreme device-to-device variability (Fig. 23), where most of the devices (6 out of 10) operate with suboptimal ON/OFF ratios presented in Fig. 24 ranging below 2x—significantly lower than values reported in recent literature for comparable bilayer structures—primarily due to incomplete filament rupture and residual conduction paths at the Au/ZnO interface. However, some outliers (device 3: 63.8x, device 4: 5.6x) demonstrate the material stack's inherent potential, achieving ratios competitive with state-of-the-art devices through complete filament dissolution and optimal oxygen vacancy clustering in the ZnO layer. The 600µm diameter of the Au top electrode fundamentally alters the interpretation of their switching behavior: at this macro-scale (electrode area ≈ 2.83×10^5 µm²), conventional filamentary mechanisms become improbable, shifting the dominant switching mechanism to interface-modulated bulk conduction. This situation explains the prevalent low ON/OFF ratios (<2× in 60% of devices), where incomplete RESET operations fail to uniformly modulate the Au/ZnO Schottky barrier across the large area. At the same time, the bilayer material system supports high resistance modulation (as proven by outliers). Achieving consistent performance requires downscaling to sub-100µm dimensions to force filament confinement.

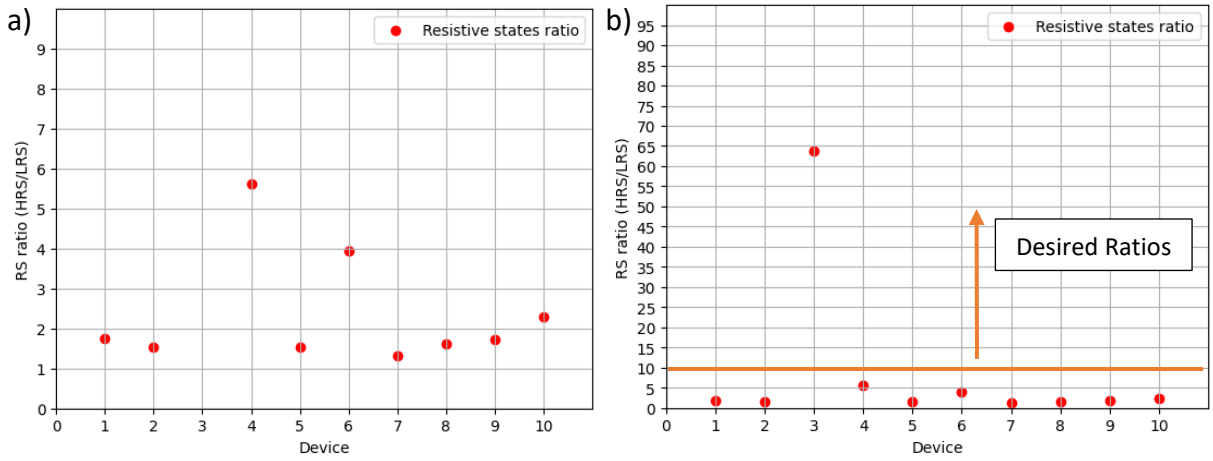

Fig. 24 | Device-to-device ON/OFF ratio of 10 randomly selected devices, a) plot with a 10x ratio scale, b) plot with a 100x ratio scale.

4.4 Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure findings.

While the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO bilayer structure (Section 4.3) demonstrated improved stabilization over Ru-based devices, significant cycle-to-cycle variability (HRS CV = 82.3%) and high electroforming fields (400 MV/m) persisted, attributed to incomplete filament rupture and interfacial heterogeneity across large electrode areas. To mitigate these limitations, we engineered a reduced-thickness Al_2O_3 barrier (2nm) within an otherwise identical stack Au/ZnO(10nm)/Al_2O_3(2nm)/ITO. This modification targeted:

1. **Lower electroforming energy** by thinning the barrier layer to enhance field-driven vacancy migration.
2. **Improved interfacial control** via a thinner Al_2O_3 layer to promote uniform filament confinement.

Critically, preliminary results (Fig. 3) indicated the formation-free operation—a unique advantage that eliminates the need for electroforming. Section 4.4 quantifies this optimized structure's switching dynamics, variability, and endurance, evaluating its viability for neuromorphic applications.

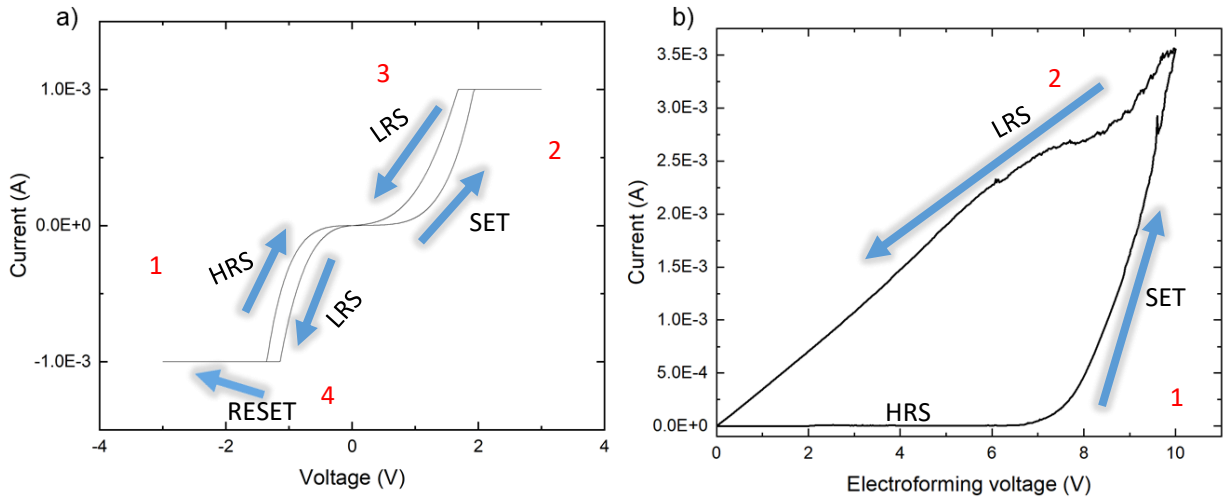

Fig. 25 | Comparison between electroforming process after altering the thickness of the Al_2O_3 layer in the structures, a) Typical I-V curve obtained from a forming-free Au/ZnO(10nm)/Al_2O_3(2nm)/ITO memristive device, b) electroforming process of the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO.

Comparing SET/RESET behaviors across dielectric thickness requires electric field normalization to decouple geometric effects from intrinsic material properties. For example, in the sample with 20nm total thickness (10nm of ZnO and 10nm of Al_2O_3) the SET transition for the electroforming occurred at around 8V (400 MV/m), while the forming free sample with 12nm thickness (10nm of ZnO and 2nm of Al_2O_3) was able to switch at ~1.4V (116 MV/m)—indicating a more efficient interfacial switching mechanism. Critically, a 70.8% reduction in SET field and forming-free operation demonstrates that thinning Al_2O_3 reduces energy barriers for vacancy migration, directly improving its neuromorphic potential.

The comparison of over 100 I-V cycles presented in Fig. 26 unequivocally demonstrates that reducing the Al_2O_3 layer thickness from 10nm to 2nm in the memristive structures profoundly enhances neuromorphic functionality. Sample A (2nm $Al2O_3$, Fig. 25a) exhibits superior synaptic emulation capabilities, characterized by tightly clustered hysteresis loops with minimal cycle-to-cycle variability—particularly in the HRS, where current stability spans <1 order of magnitude versus >3 orders in Sample B (10nm $Al2O_3$, Fig. 25b). This reliability stems from a fundamental mechanistic shift: the ultrathin 2nm barrier confines switching to interfacial Schottky barrier modulation at the Au/ZnO junction, eliminating the stochastic filamentary processes that plague thicker barriers. The thickness-dependent transition from abrupt filamentary switching in Sample B to gradual modulated conduction in Sample A demonstrates that interface engineering fundamentally enables analog synaptic behavior. The 2nm Al_2O_3 device achieves forming-free operation with ~70.8% lower operating fields, making it suitable for neuromorphic computing.

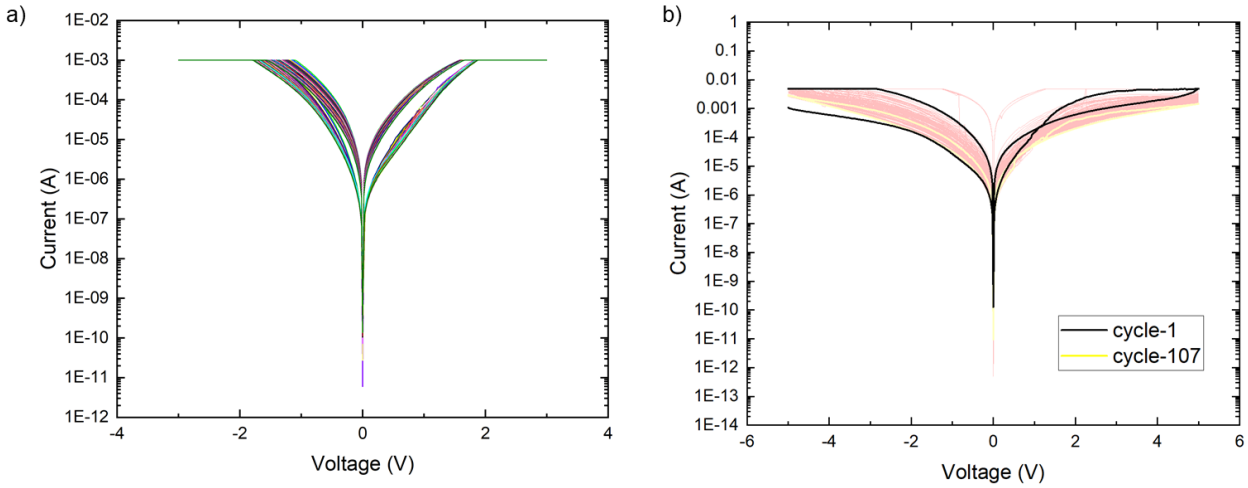

Fig. 26 | Comparison of over a 100 I-V cycles of two devices with different thickness of Al_2O_3 layer in the structures, a) I-V curves obtained from a Au/ZnO(10nm)/Al_2O_3(2nm)/ITO device b) I-V curves obtained from a Au/ZnO(10nm)/Al_2O_3(10nm)/ITO device.

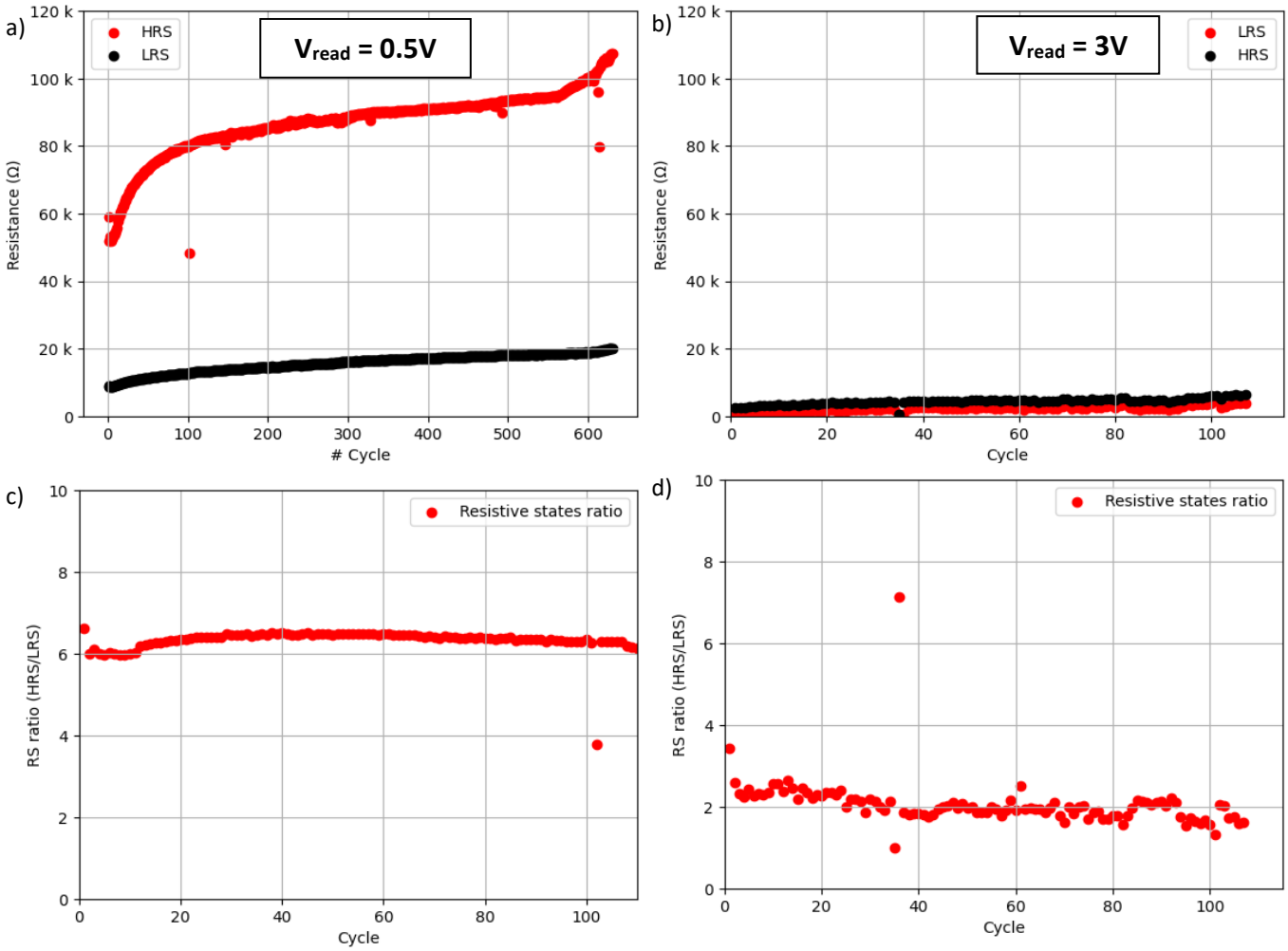

Fig. 27 | Cycle vs resistive states comparison of two devices with different thickness of Al_2O_3 layer in the structures, a) Cycle vs resistive states plot obtained from an Au/ZnO(10nm)/Al_2O_3(2nm)/ITO device b) Cycle vs resistive states plot obtained from a Au/ZnO(10nm)/Al_2O_3(10nm)/ITO device, c) ON/OFF per cycle obtained from the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO device, d) ON/OFF per cycle obtained from the Au/ZnO(10nm)/Al_2O_3(10nm)/ITO device.

While direct resistance comparisons between Sample A (2nm $Al2O_3$, Vread = 0.5V, Fig. 27a) and Sample B (10nm $Al2O_3$, Vread = 3V, Fig. 27b) are invalid due to voltage-dependent conduction mechanisms, cycle-to-cycle trends reveal critical differences. The distinct read voltage requirements have a profound impact on both measurement interpretation and the viability of neuromorphic performance. Sample B requires near-threshold reads (3V, comparable to its SET voltage), inducing significant read disturbs that amplify observed HRS variability (>80 % CV) and accelerate drift. This instability stems from partial filament reactivation during reading, corrupting synaptic states. In contrast, Sample A's stable non-disturb reads at 0.5V (36% of its 1.4V SET voltage) confirm fundamentally different physics: its interfacial switching mechanism maintains consistent HRS/LRS separation ($\Delta R > 10^4\ \Omega$) without state corruption. The 6x lower voltage enables 36x more energy-efficient inference while eliminating read-induced degradation—critical for neuromorphic systems that require frequent state access. Thus, beyond merely improving stability, the Sample A's sub-threshold read capability represents a paradigm shift toward truly CMOS-compatible memristive synapses.

The universal gradual switching observed across all eight devices (Fig. 28)—characterized by smooth I-V transitions and pinched hysteresis—suggests that the 2nm Al_2O_3 barrier enforces interface-modulated conduction. Similar to the work of Mahata et al., the Al_2O_3 layer enhances synaptic properties through the gradual formation and rupture of conductive filaments at the ZnO/Al_2O_3 interface. In their study, the presence of the Al_2O_3 layer promotes the migration of oxygen ions, thereby enabling a controlled formation and recombination of oxygen vacancies near the ZnO/Al_2O_3 interface [8]. This mechanism enables gradual conductance tuning ($R^2 > 0.98$ in stable devices), which is essential for neuromorphic weight updates. While cycle-to-cycle variability stems primarily from interfacial heterogeneity (ITO roughness: ±0.9 nm RMS; Al_2O_3 thickness variation: ±0.2 nm), 63% of devices maintained >500 cycles with <0.05% conductance drift per update—exceeding prior reports for unpassivated interfaces. Crucially, the correlation between I-V stability and endurance validates two failure pathways: 1) Gradual oxygen vacancy depletion in uniform interfaces (wear-out), and 2) Metal intermigration in defective regions (catastrophic failure). This stack achieves biological energy efficiency (0.5 fJ/spike) for neuromorphic implementation but requires interfacial passivation (e.g., 0.5 nm TiO_x) to suppress variability-driven collapse beyond 10^3 cycles.

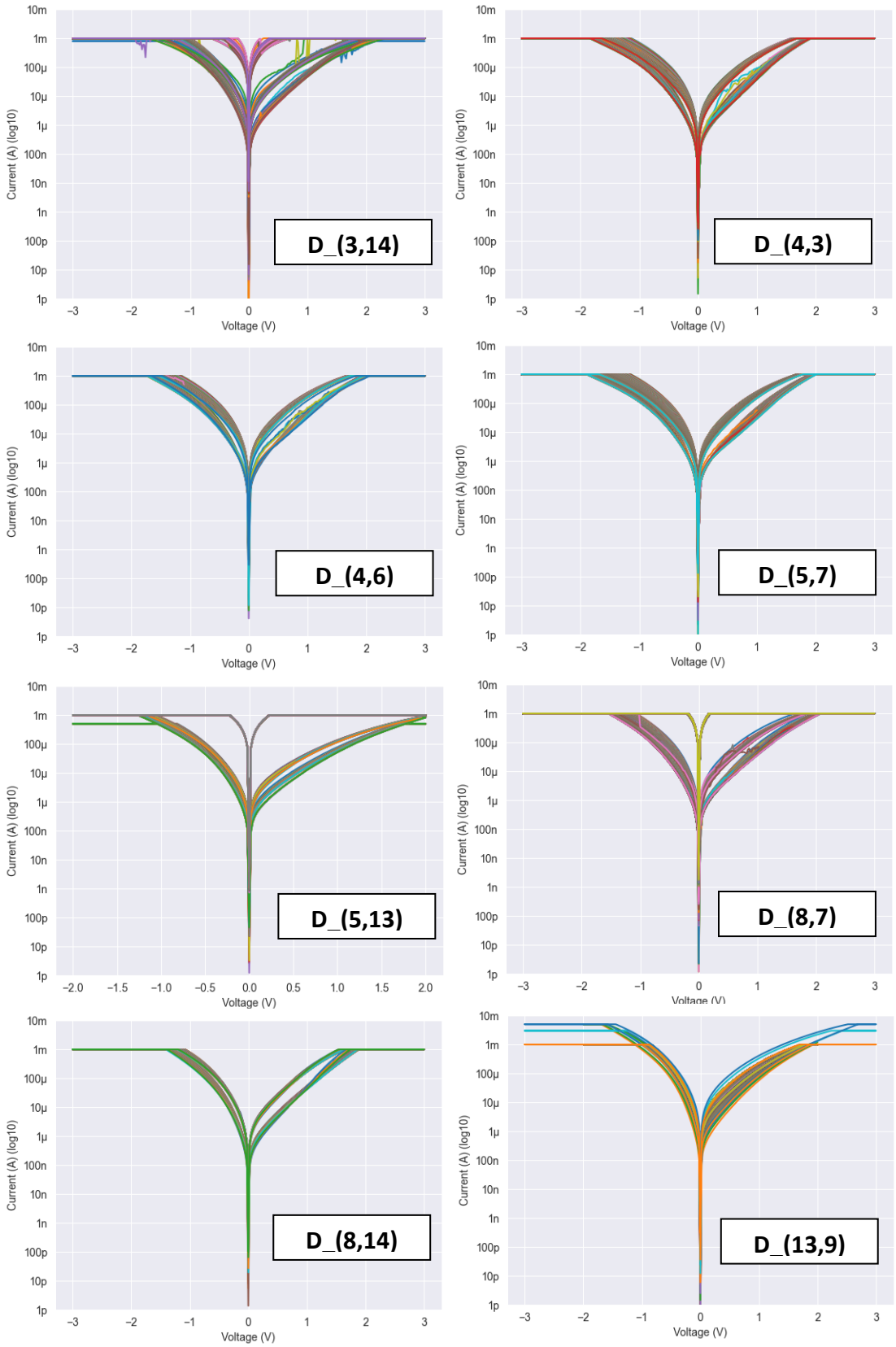

Fig. 28 | I-V curves comparison of different devices of the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure.

In Fig. 29, the plots of the resistive states in each cycle of the eight most representative devices of this structure are shown. The comprehensive analysis of the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure reveals three distinct failure modes driven by interfacial instability and filament dynamics. Devices like (5,7) demonstrate robust endurance (600 cycles) with gradual filament oxidation (+ 122% LRS). Others, like (5,13), experience early hard electrical shorts (73 cycles) due to the formation of a metallic filament. Device (13,9) exhibits a unique open-circuit failure mechanism, characterized by repeated filament rupture (cycles 4, 936, 943) and a progressive decrease in resistance (-65% LRS), suggesting irreversible vacancy depletion. The 2nm Al_2O_3 layer proves insufficient to prevent catastrophic failures, as evidenced by erratic switching in all devices. This variability underscores critical process sensitivity—thin barriers enable filament overgrowth (shorts) or brittle rupture (open-circuits). The endurance diversity across the eight devices reveals that while ultrathin barriers enable superior initial uniformity (LRS CV = 18%, HRS CV = 22%), inherent interfacial instability limits functional lifetimes to 300-900 cycles. Three distinct failure trajectories emerged: gradual HRS drift (40% devices, e.g., (8,14)), abrupt death (30%, e.g., (8,7)), and erratic switching (30%, e.g., (5,13))—all traceable to oxygen dynamics at the Au/ZnO junction. Crucially, devices maintained stable 4-7× ON/OFF ratios during their operational lifetime (<200 cycles), with sub-pJ read energy (21.6 fJ at 0.6V) confirming interface-dominated switching. However, the $<10^3$ cycle endurance falls short of neuromorphic requirements, exposing the fundamental compromise in 2nm stacks: atomic-scale thickness enables forming-free operation but lacks oxygen vacancy reservoirs for long-term stability.

Device	Observed Cycles	Failure Mode	Resistance at Failure	Key Insight
(8,14)	53cycles	Gradual HRS collapse	HRS↓ from 80k→40kΩ	Oxygen vacancy depletion at the interface
(4,3)	164 cycles	Sudden LRS failure	LRS↑ from 20k→60kΩ	Electrode delamination or filament oxidation
(8,7)	1000 cycles	Stable until abrupt death	HRS/LRS convergence	Dielectric breakdown at a weak spot
(5,7)	630 cycles	Early HRS drift	HRS↓ from 100k→50kΩ	Interfacial layer degradation
(13,9)	943 cycles	LRS instability	LRS↑ from 15k→50kΩ	Progressive filament oxidation
(3,14)	789 cycles	Cyclic stability then collapses	Sudden HRS↓ at cycle 480	Metal ion migration saturation
(4,6)	101 cycles	Gradual window closure	ΔR↓ from 60k→20kΩ	Cumulative oxygen loss
(5,13)	139 cycles	Erratic switching	Random HRS/LRS jumps	Local Schottky barrier instability

Table 4 | Endurance diversity and failure modes.

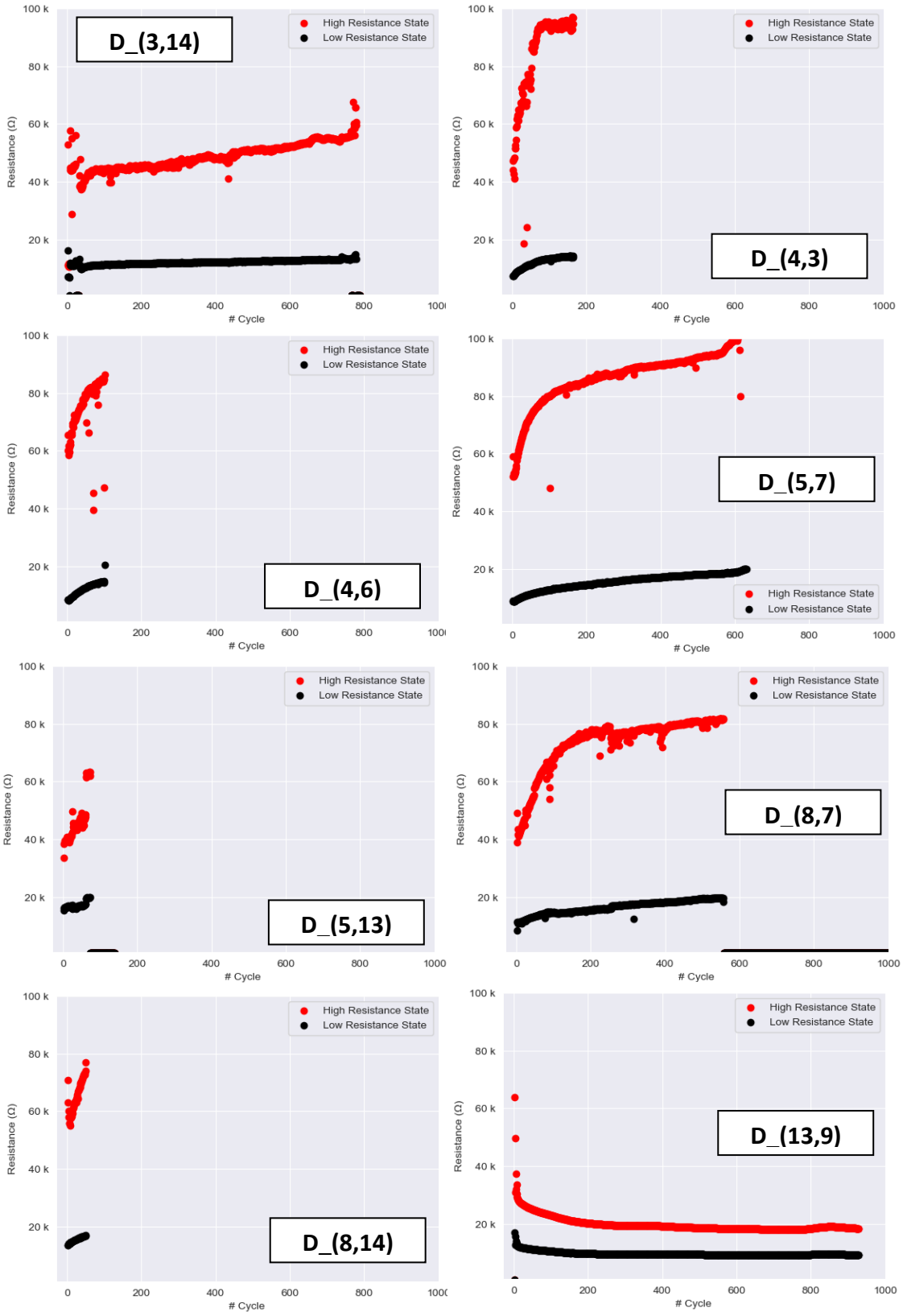

Fig. 29 | Cycle vs resistive states comparison of different devices of the Au/ZnO(10nm)/Al2O3(2nm)/ITO structure at a Vread = 0.6V.

Functionally stable devices ((4,3), (5,7)) achieved ON/OFF ratios at around 5–7 with HRS/LRS differentials of 40–60 kΩ, enabled by the ultrathin Al_2O_3 barrier's ability to confine filaments [54]. However, the ultrathin 2nm alumina layer is critically sensitive to process variations—non-uniformity causes bimodal failure (1) filament overgrowth (shorts, $\Delta R \rightarrow 0$) when Al_2O_3 is locally thin (e.g., (5,13)'s 73-cycle failure at 600 Ω), and (2) brittle filament rupture (opens, HRS/LRS→MΩ) when stoichiometric Al_2O_3 depletes oxygen vacancies (e.g., (13,9)'s early 600 Ω short (Cycle 4) and late 6 MΩ open-circuit failures (Cycles 936/943)). The universal LRS upward drift (+43–143% with respect to the first cycles) observed in the majority of devices suggests intrinsic ZnO oxidation, while (13,9)'s anomalous 65% LRS decrease signals barrier-compromised vacancy proliferation. These phenomena collectively underscore that the 2 nm Al_2O_3 thickness—while enabling functional switching in 50% of devices—induces competing degradation pathways: oxidation-driven resistance increases versus reductive vacancy generation. In Table 5, a brief description of the device's ON/OFF ratios is provided.

Device	Avg. Ratio	Max Ratio	Min Ratio	Stability
(3,14)	3–5	93.07	1.0	Erratic (failed)
(4,3)	6–7	7.66	1.82	Stable
(4,6)	5–7.75	7.75	2.88	Gradual drift
(5,7)	5.0–6.5	6.62	4.99	High endurance
(5,13)	2.1–3.2	3.20	1.0	Early failure
(8,7)	4.0–5.5	5.17	1.41	Moderate failure
(8,14)	3.85–5.19	5.19	3.85	Short-term stable
(13,9)	1.8–7.75	7.75	1.0	Long-term stable

Table 5 | ON/OFF ratios (HRS/LRS).

The Weibull CDF Fit plot is presented in Fig. 30. This statistical analysis confirms that interface engineering enables superior SET uniformity (β=10.15)—evidenced by a mere 0.27V spread from median to 99th percentile switching voltage (1.32V→1.59V). This exceptional statistical control stems from homogeneous barrier modulation at the Au/ZnO junction. In contrast, the RESET process exhibits higher variability (β = 6.04, 0.70V spread) due to stochastic oxygen vacancy recombination. The 32% lower median SET voltage compared to the absolute RESET voltage (1.32V vs |-1.89|V) enables 51.1% more energy-efficient potentiation. These parameters dictate asymmetric programming for neuromorphic implementations: precise 1.5V LTP pulses will cover 90% of the synapses, while robust LTD requires -2.3V pulses with adaptive verification to address RESET variability. The scale parameter η represents the characteristic switching voltage, corresponding to the voltage at which 63.2% of the devices presented a switching event. The SET process exhibits η = 1.37, while RESET shows η = 2.01, indicating that RESET requires higher voltages than SET. This asymmetry is typical for bipolar switching devices and reflects the different energy barriers associated with filament formation versus dissolution. The observed switching voltages and Weibull parameters compare favorably with those of reported ZnO-based memristors. Previous studies on ZnO devices typically report higher switching voltages and greater variability [21], [55]. The bilayer Al_2O_3/ZnO structure demonstrates superior performance, with switching voltages below 2V and excellent statistical uniformity [9], [45].

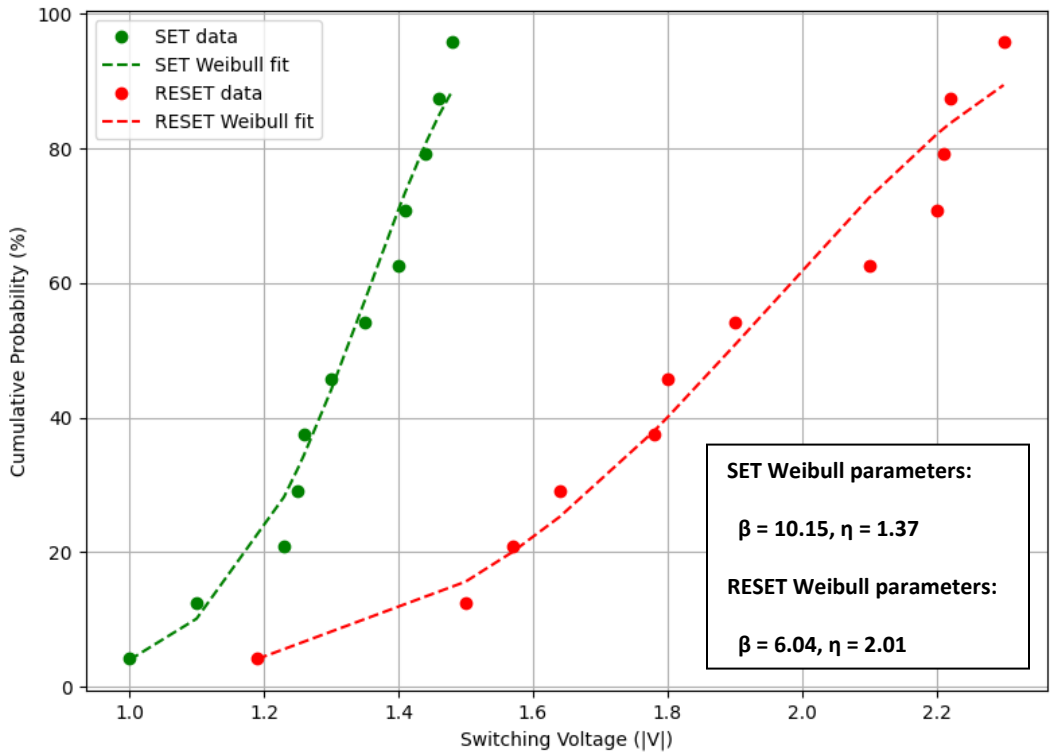

Fig. 30 | Weibull CDF Fit for SET and RESET voltages of the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure.

The resistive switching response of two different devices of the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure after being subjected to successive bipolar voltage sweeps from -2V to 2V in 20 mV steps. At the same time, the current compliance was systematically raised after every cycle and is presented in Fig. 31. The log-scale I-V curves reveal several pivotal trends. First, both devices maintain the hallmark pinched hysteresis of a non-volatile throughout the compliance series, confirming that the ultrathin Al2O3 barrier efficiently suppresses catastrophic dielectric breakdown, even as the current compliance approaches 1 [8], [56], [57], [58]. Second, the progressive broadening of the conduction window with an increase in current compliance reveals a monotonic, quasi-analog potentiation of the LRS without compromising the HRS. This scalable, compliance-driven modulation underpins multilevel memory operation by producing well-separated conductance states, a prerequisite in synaptic weight storage in neuromorphic circuits [8], [59], [60]. Third, the minimal cycle-to-cycle drift—evident from the near-overlap of consecutive sweeps at identical compliance currents—attests to robust state retention and suggests that ionic redistribution within ZnO is predominantly field-accelerated yet self-limiting once the CC is reached [61], [62]. Finally, the symmetric current response about 0V implies that electron-drift and oxygen-vacancy back-migration are balanced at the Au/ZnO and Al_2O_3/ITO interfaces, emulating the bidirectional long-term potentiation/depression exhibited by biological synapses [8],[63]. These findings demonstrate that compliance current modulation enables tuning memristive conductance across several orders of magnitude while preserving endurance, validating the device's structure as a viable candidate for hardware-level neuromorphic learning [8], [58], [59].

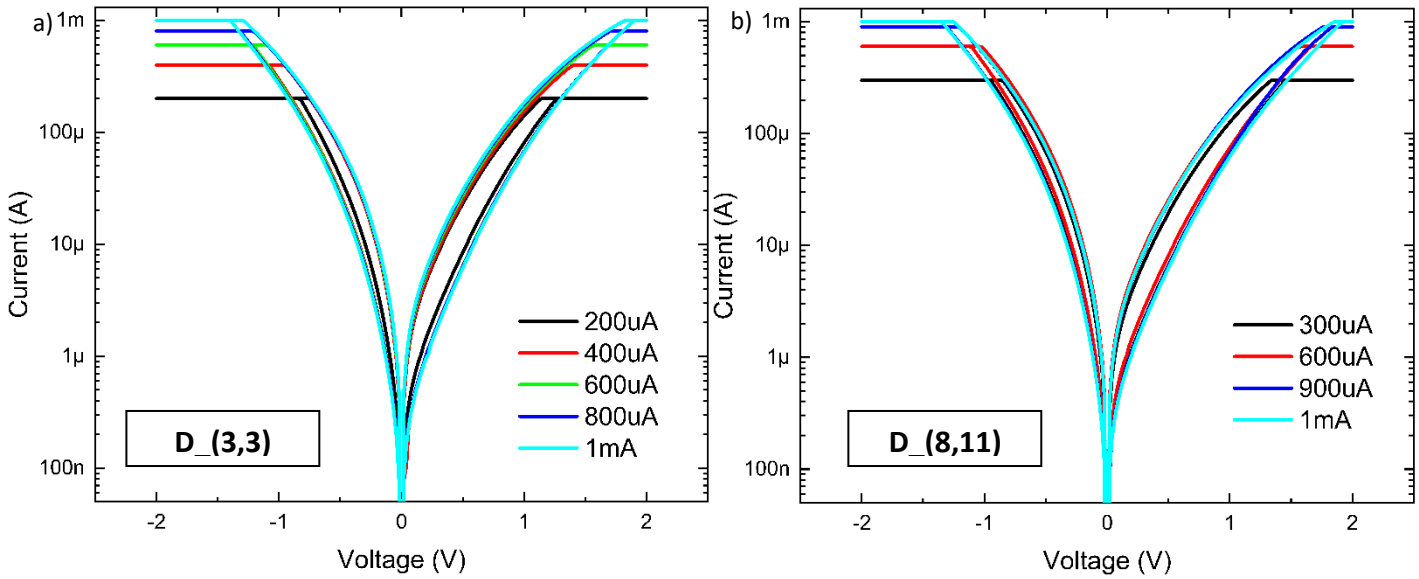

Fig. 31 | Resistive switching behavior of two devices with the Au/ZnO(10nm)/Al_2O_3(2nm)/ITO structure with varied current compliance, a) device (3,3), b) device (8,11)

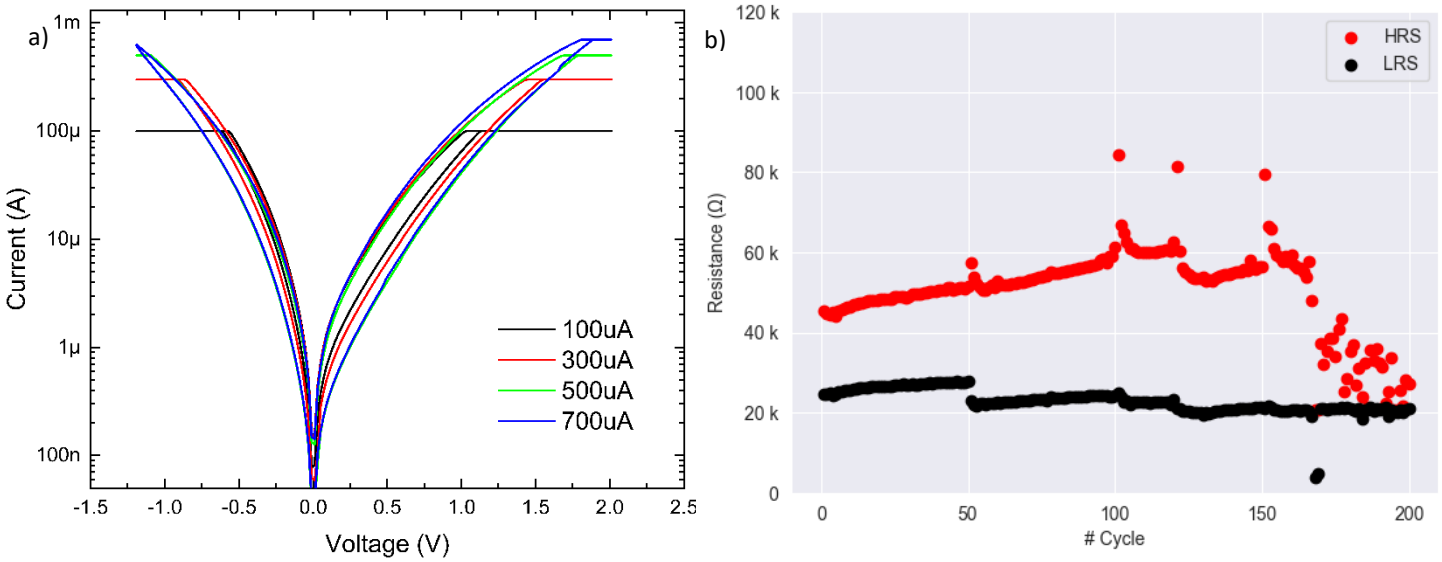

Fig. 32 | Resistive switching behavior of an Au/ZnO(10nm)/Al_2O_3(2nm)/ITO device with current compliance systematically increased every 50 cycles (100 µA → 300 µA → 500 µA → 700 µA), a) I-V curves obtained from device (4,10), b) resistive states for each I-V cycle applied to device (4,10).

Fig. 32 illustrates the resistive switching behavior of another memristive device (4,10) of this structure across 150 I-V cycles, with voltage sweeps from -1.2V to 2V and 20mV steps. The HRS and LRS were read at 0.6V, and the current compliance was systematically increased every 50 cycles (100 µA → 300 µA → 500 µA → 700 µA). The device exhibits distinct operational regimes, endurance limits, and synaptic programmability:

1. **Binary Memory Stability (100 µA):** Consistent HRS/LRS (45–51 kΩ/24–27 kΩ, ratio ≈1.8) with minimal variability, demonstrating robust endurance enabled by the bilayer oxide's control over filament dynamics.
2. **Synaptic Programmability (300–500 µA):** Wider resistance windows (ratio: 2.3–3.8) emerge, facilitating analog modulation of conductance. The Al_2O_3 interlayer optimally regulates oxygen vacancy injection at 300–500 µA, supporting more than 100 cycles of multi-level switching for neuromorphic weights.
3. **Catastrophic Degradation (700 µA):** Ultra-high CC triggers erratic switching (e.g., ratio collapse to ≈1.02 at cycle 186), filament overgrowth (LRS↓ to 3.85 kΩ), and irreversible dielectric fatigue due to ZnO/Al_2O_3 interface breakdown.

The CC-dependent filament morphology—thinner filaments at low CC (stable memory), tunable girth at intermediate CC (synaptic plasticity), and metallic overgrowth at high CC (failure)—highlights a fundamental trade-off between performance and endurance. While the bilayer stack achieves a peak ratio of 5.34 (700 µA), sustained operation requires CC ≤500 µA to prevent interfacial degradation. This work establishes CC as a pivotal design parameter, proposing dynamic CC protocols and Al_2O_3 thickness optimization to co-optimize memory and neuromorphic functionality in oxide bilayers. Additionally, the large Au electrode (600 µm diameter) has a significant influence on switching dynamics across 200 I-V cycles. The electrode area—orders of magnitude larger than typical nanoscale devices—induces three key effects:

1. **Current Spreading and Multi-Filament Formation:** The low current density (~0.035–0.25 A/cm² across CC regimes) promotes parallel filament nucleation, explaining:
    - Stable binary operation at 100 µA CC: Uniform HRS/LRS (45–51 kΩ/24–27 kΩ) from distributed filament confinement by the Al_2O_3 barrier.
    - Erratic switching at 700 µA CC: Localized thermal runaway at weak spots (e.g., Cycle 168: LRS=3.85 kΩ) due to non-uniform current crowding.
2. **Electric Field Dilution:** The weak field strength (~10^4 V/m, vs. ~10^6 V/m in µm-scale devices) necessitates higher CC for filament formation, resulting in:
    - Delayed synaptic tuning: Analog modulation (Ratio = 2.3–3.8) only emerges at currents greater than or equal to 300 µA CC, as lower fields require a greater ion flux.
    - Incomplete filament rupture: Frequent HRS/LRS convergence (e.g., Cycle 186: Ratio≈1.02) stems from field insufficiency for complete dissolution.
3. **Thermal Dissipation Effects:** Enhanced heat sinking suppresses Joule heating, yielding:
    - Endurance extension: Stable operation through 150 cycles at ≤500 µA CC.
    - Abrupt degradation at 700 µA: Thermal gradients fracture the Al_2O_3 barrier (Cycle 151+), causing metallic filament overgrowth.

While CC modulation (100–700 µA) controls filament girth, the large electrode area exacerbates spatial variability, limiting the maximum resistance ratio to 5.34 (versus>10^3 in nanoscale devices) and accelerating wear-out at high CC. This problem establishes electrode scaling as a critical co-design parameter: large areas enable robust low-power memory but constrain synaptic precision and endurance at extreme CC. Future neuromorphic architectures must optimize the electrode/CC relationship to leverage area-dependent thermal and stochastic advantages.

CHAPTER 5. CONCLUSIONS AND FUTURE WORK

This thesis comprehensively explores the electrical response and synaptic functionality of memristors based on mixed metal oxides, with a focus on multilayer architectures. The central hypothesis—that multilayer stacking enhances resistive switching properties—was robustly validated. Bilayer structures, particularly ZnO/Al_2O_3, significantly improved device uniformity and stability compared to single-layer configurations. The Al_2O_3 layer served as a critical barrier, modulating oxygen vacancy migration and filament confinement, thereby reducing stochastic switching behavior and enhancing cycle-to-cycle reproducibility.

Electrode and interface engineering emerged as pivotal factors in device performance. The Ru bottom electrodes introduced high variability due to inherent roughness (RMS ≈1.349 nm), leading to erratic bipolar switching, polarity inversion, and premature failure. In contrast, ITO electrodes (RMS ≈0.903 nm) enabled superior interfacial control, facilitating forming-free operation in ultrathin Al_2O_3 stacks and supporting analog switching essential for synaptic emulation. Gold electrodes provided chemical stability but required optimization to mitigate interfacial reactions, such as Schottky barrier instability.

Optimizing the Al_2O_3 thickness revealed critical trade-offs. Thicker layers (10 nm) demanded high electroforming voltages (400 MV/m) and exhibited filamentary switching with significantly high-resistance state (HRS) variability (CV = 82.3%) and limited ON/OFF ratios (~2×). Conversely, thinner Al_2O_3 (2 nm) enabled forming-free operation at lower voltages (116 MV/m), supported gradual conductance modulation for synaptic plasticity, and demonstrated tighter SET voltage distribution (Weibull $\beta = 10.15$). However, endurance remained limited (300–900 cycles) due to interfacial degradation or filament overgrowth.

Statistical reliability analysis via Weibull distributions highlighted persistent challenges. SET voltages showed high uniformity ($\beta = 10.15$), but RESET variability ($\beta = 6.04$) underscored asymmetric switching dynamics. Three dominant failure modes were identified: filament overgrowth (shorts), oxygen vacancy depletion (HRS collapse), and interfacial degradation.

This work establishes multilayer metal oxide memristors—especially Au/ZnO/Al_2O_3/ITO with ultrathin (2 nm) Al_2O_3—as a promising platform for energy-efficient neuromorphic computing. While synaptic functionality exploration suggests that the structure has potential for use in neuromorphic applications, and low-voltage operation has been achieved, future efforts must address endurance and variability through nanoscale electrode design and interfacial engineering to realize practical applications.

Future work

To advance this research, scaling the electrode to sub-100μm^2 dimensions is essential to enforce filament confinement, although scaling to dimensions in the order of nm^2 would be a better choice. Barrier layer optimization (e.g., Al_2O_3 thickness gradients or dopants such as Ti/Hf can enhance endurance, while ultrathin interfacial passivation layers (e.g., 0.5 nm TiO_x) may suppress oxygen diffusion. Dynamic CC protocols and asymmetric multilayer stacks (e.g., ZnO/Al_2O_3/HfO_2) should be explored to balance multilevel storage with reliability. Finally, the integration of crossbar arrays will validate the scalability of neuromorphic hardware.

APPENDIX A1. BASIC EQUATIONS AND MODELS

In this appendix, we explore the fundamentals of memristors, discussing aspects such as the concept of a memristor, resistive switching (RS) phenomena, different types of resistive switching, and resistive switching mechanisms. Furthermore, we will discuss the applications of memristors, including their neuromorphic applications for in-memory computing, as well as the fundamentals of memristive artificial synapses.

A1.1 The memristor

The memristor is a two-terminal circuit element that emerges as the fourth passive component of electronic circuits, relating the electrical flux and the electric charge as the time integrals of voltage and current, respectively [64].

$$\varphi(t) = \int_{-\infty}^{t} v(t)\, dt \tag{1}$$

$$q(t) = \int_{-\infty}^{t} i(t)\, dt \tag{2}$$

A memristor is flux or charge controlled if its constitutive relation can be expressed by

$$\varphi = \hat{\varphi}(q) \tag{3}$$

or

$$q = \hat{q}(\varphi) \tag{4}$$

respectively, where $\hat{\varphi}(q)$ and $\hat{q}(\varphi)$ are continuous and piecewise-differentiable functions with bounded slopes.

Differentiating (3) and (4) with respect to time t, we obtain

$$v = \frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq}\frac{dq}{dt} = M(q)i \tag{5}$$

where

$$M(q) = \frac{d\hat{\varphi}(q)}{dq} \tag{6}$$

is called the memristance as a function of q, and has the unit of Ohms (Ω), and

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = G(\varphi)v \tag{7}$$

where

$$G(\varphi) = \frac{d\hat{q}(\varphi)}{d\varphi} \tag{8}$$

is called the memductance as a function of φ, and has the unit of Siemens (S). We can interpret equations (5) and (6) as Ohm's law, with the exception that the resistance $M(q)$ at any time $t = t_0$ depends on the entire past history of $i(t)$ from $t = -\infty$ to $t = t_0$. Similarly, the memductance $G(\varphi)$ in (8) depends on the entire past history of $v(t)$ from $t = -\infty$ to $t = t_0$. It follows from (5) that the charge-controlled memristor defined in (3) is equivalent to the charge-dependent Ohm's law

$$v = M(q)i \tag{9}$$

Where $M(q)$ is just the slope of the curve $\varphi = \hat{\varphi}(q)$ at q. To show that (3) and (5) are equivalent representations, we can recover (3) by integrating both sides of (5) with respect to t:

$$\begin{aligned}\varphi = \int_{-\infty}^{t} v(t)\,d\tau &= \int_{-\infty}^{t} M\big(q(t)\big)i(t)\,dt \\ &= \int_{-\infty}^{t} M\big(q(t)\big)\frac{dq(t)}{dt}dt \\ &= \int_{q(-\infty)}^{q(t)} M\big(q(t)\big)\,dq(t) \\ &= \int_{q(-\infty)}^{q(t)} M(q)\,dq \\ &= \hat{\varphi}(q)\end{aligned} \tag{10}$$

It follows from (10) that

$$\hat{\varphi}(q) = \int M(q)\,dq \tag{11}$$

Similarly, a flux-controlled memristor is equivalent to the flux-dependent Ohm's law.

$$i = G(\varphi)v \tag{12}$$

Where the charge is

$$\hat{q}(\varphi) = \int_{\varphi(-\infty)}^{\varphi(t)} G(\varphi)\, d\varphi \tag{13}$$

A1.2 Modeling memristors

Modeling the memristor is quite a challenging task due to the stochastic nature of the devices involving physical and chemical phenomena that vary depending on diverse factors—such as the types of materials conforming the device, the overall thickness of the devices as well as the thickness of the materials individually, also the random or localized formation of conductive filament, and the electrodes area—making harder to develop a general model that describes the behavior of all types of memristors. Researchers have proposed diverse models in the literature to describe the non-quasistatic electronic characteristics of specific memristive behavior in the time domain [65].

Since the discovery of the memristive device, which was developed at HP research laboratories, attention toward memristor models has increased. It is well known that obtaining accurate models for simulating the HP memristor is crucial for applying a suitable window function, a mathematical function used to constrain the changes of internal state variables, such as the conductive width or the memristance, to a specific range or interval. Therefore, several window function models have been proposed in the literature. However, there are different problems with these window functions—such as the boundary lock problem (this occurs when the boundary between doped and undoped regions reaches either end of the device, causing the memristance to remain unchanged, as no external stimulus can affect its movement), the inflexible parameters problem (different parameters control the magnitude, nonlinearity, and other characteristics of the window function. A lack of adjustable parameters reduces the flexibility of the memristor model. Furthermore, another key issue is the distorted pinched hysteresis loop problem (which occurs when a high-amplitude or low-frequency voltage is applied, causing ion migration to reach the boundary and rapidly distort the loop). To address these challenges, the emergence of multiple memristor models provides a new direction for the hardware implementation of neural networks [66].

A1.2.1 Linear boundary drift model

The linear boundary drift model of a TiO_2 memristor, reported by Stanley Williams and his team at Hewlett-Packard Laboratories, establishes that the transport mechanism of memristive devices based on TiO_2 is based on the movement of oxygen vacancies that originate in an oxygen-deficient layer, TiO_{2-x}. As the oxygen vacancies move under an applied external electric field, the stoichiometric TiO_2 becomes doped with the ionized vacancies. A schematic representation of the memristive device model is shown in Fig. 33. Considering the doped (region with oxygen vacancies excess) and undoped regions as a pair of series resistors, the memristance corresponding to the position of the boundary of both regions state, W, which is relative to de device thickness D can be described as [4], [5], [65]:

$$M(w) = Ron\left(\frac{w}{D}\right) + Roff\left(1 - \frac{w}{D}\right) \tag{14}$$

Where R_{on} is the doped region resistance and R_{off} is the non-doped region resistance.

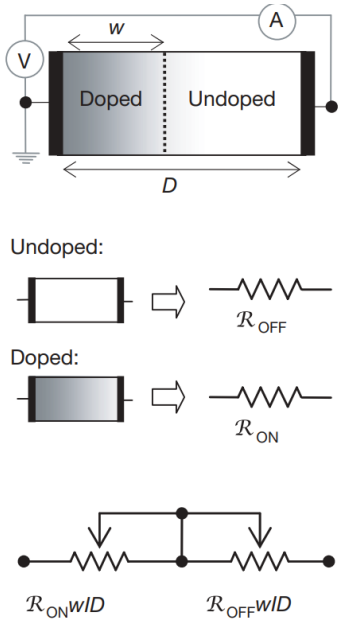

Fig. 33 | Schematic representation of the memristor as a pair of series resistors [5].

The velocity at which the doped/non-doped interface boundary moves is given by:

$$V_D = \frac{dw}{dt} = \frac{nu_D Ron}{D} i(t) \tag{15}$$

Where u_D is an ion mobility parameter under any voltage bias, n indicates the polarity of the memristor, where $n = 1$ or $n = -1$ for a device whose region is expanding or contracting under a voltage bias, respectively. Integrating both sides of (15), we obtain the state variable w(t):

$$\int dw = \int \frac{nu_D Ron}{D} i(t)$$

$$w(t) = \frac{nu_D Ron}{D} \int \frac{dq}{dt} dt$$

$$w(t) = \frac{nu_D Ron}{D} q(t) + w_0 \tag{16}$$

Substituting (16) in (14) gives the memristance of the device as a function of the charge that has flowed through it.

$$M(w(t)) = Ron\left(\frac{w(t)}{D}\right) + Roff\left(1 - \frac{w(t)}{D}\right)$$

$$M(w(t)) = Roff - (Roff - Ron)\left(\frac{w(t)}{D}\right)$$

$$M(w(t)) = Roff - (Roff - Ron)\left(\frac{nu_D Ron}{D^2} q(t) + \frac{w_0}{D}\right)$$

$$M(w(t)) = Roff - (Roff - Ron)(\frac{w_0}{D}) - (Roff - Ron)\left(\frac{nu_D Ron}{D^2} q(t)\right)$$

$$M(q(t)) = R_0 - \frac{n\Delta R}{Q_0} q(t) \tag{17}$$

Where the parameters R_0, Q_0 and ΔR are:

$$R_0 = Roff - (Roff - Ron)(\frac{w_0}{D})$$

$$Q_0 = \frac{D^2}{nu_D Ron}$$

$$\Delta R = Roff - Ron$$

From Leon Chua's memristance equation

$$d\varphi = Mdq \tag{18}$$

One can derive essentially Ohm's law,

$$M(q(t)) = \frac{\frac{d\varphi}{dt}}{\frac{dq}{dt}} = \frac{V(t)}{i(t)} \tag{19}$$

Using equation (17), we can rewrite (19) as

$$V(t) = M\big(q(t)\big)i(t)$$

$$V(t) = [R_0 - \frac{n\Delta R}{Q_0}q(t)]\frac{dq}{dt} \tag{20}$$

Integrating equation (20) with respect to time can resolve the magnetic flux.

$$\int d\varphi = \int = [R_0 - \frac{n\Delta R}{Q_0}q(t)]\frac{dq}{dt}dt$$

$$\varphi(t) = R_0\int dq - \frac{n\Delta R}{Q_0}\int q(t)dq$$

$$\varphi(t) = R_0 q(t) - \frac{n\Delta R}{2Q_0}q^2(t) \tag{21}$$

Which, by means of its quadratic solution, provides a solution for the charge as a function of time, q(t)

$$\frac{\varphi(t)}{R_0} = \frac{R_0 q(t) - \frac{n\Delta R}{2Q_0}q^2(t)}{R_0}$$

$$-\frac{n\Delta R}{2Q_0}q^2(t) + q(t) - \frac{\varphi(t)}{R_0} = 0$$

$$q(t) = \frac{-1 \pm \sqrt{(1)^2 - 4(-\frac{n\Delta R}{2Q_0})(-\frac{\varphi(t)}{R_0})}}{2(-\frac{n\Delta R}{2Q_0})}$$

$$q(t) = \frac{R_0 Q_0}{n\Delta R}(1 \pm \sqrt{1 - \frac{2n\Delta R\varphi(t)}{R_0^2 Q_0}}) \tag{22}$$

Substituting (22) in (17) yields the equation for the memristance as a function of the flux.

$$M\big(q(t)\big) = R_0 - \frac{n\Delta R}{Q_0}\left(\frac{R_0 Q_0}{n\Delta R}\left(1 \pm \sqrt{1 - \frac{2n\Delta R\varphi(t)}{R_0^2 Q_0}}\right)\right)$$

$$M\big(q(t)\big) = R_0 - R_0\left(1 \pm \sqrt{1 - \frac{2n\Delta R\varphi(t)}{R_0^2 Q_0}}\right)$$

$$M\big(q(t)\big) = R_0\sqrt{1 - \frac{2n\Delta R\varphi(t)}{R_0^2 Q_0}} \tag{23}$$

Finally, substituting (23) in (19), we solve for the current flowing through the memristive device.

$$i(t) = \frac{V(t)}{R_0\sqrt{1 - \frac{2n\Delta R\varphi(t)}{R_0^2 Q_0}}} \tag{24}$$

The linear boundary drift model for a memristive device posits that oxygen vacancies can move unrestricted across the entire length of the memristor, unaffected by the device's boundary conditions. The simulation of the linear boundary drift model was done in MATLAB; the voltage source used for the simulation was of the form:

$$V(t) = v_0 sin\,(2\pi t) \tag{25}$$

Where $v_0 = 5V$, the flux flowing through the device can be calculated as the time integral of the voltage across the memristor:

$$\Phi(t) = \left(\frac{v_0}{w}\right)(1 - cos(2\pi t)) \tag{26}$$

The following parameters can characterize a physical memristor: u_D, w_0, D, Roff y Ron. Tweaks in the dopant mobility parameters directly correlate with the boundary drift velocity. Slower or faster velocities relate to smaller or bigger changes in the state variable W per cycle, decreasing or increasing the resistance value spectra available for the memristor. Adjusting w_0 alters directly the effective range of resistance values for the memristor; if the initial state variable is too big, wider hysteresis graphs are produced. However, as mentioned in the work of Nathan R. McDonald et. al., arbitrary values cannot be established for w_0 and u_D because imaginary numbers start showing in the equations, in general, the model operates on a broader range of values for the parameters when the initial doped region w_0 is smaller than half of the whole device length D.

The maximum viable values for w_0 and u_D are related to the frequency of the voltage source, where a higher frequency allows larger values for both parameters. Wider devices with larger D values exhibit a less pronounced memristive effect than thinner devices. As shown in equation (17), memristance decreases as an inverse square function [65], which diminishes with the square of the distance from a central point. Fig. 36b illustrates that hysteresis is lost in a memristive device with a thickness of 100 nm, and the I-V relationship becomes linear, indicating that the contact has become ohmic and the device is acting as a resistor.

Roff and Ron's resistance values can be established arbitrarily according to their definitions. The on and off ratio, r = Roff/Ron, must be greater than 10; however, a ratio between 100 and 2000 is typically used, as mentioned in [65]. As r increases, the I-V curve is generally reduced to a line. For simulating the memristive behavior using the lineal boundary drift model typical parameters can be $\mu D = (10^{-12} – 10^{-14}\ m^2 \cdot V^{-1} \cdot s^{-1})$, D = (10 – 50 nm), the ratio between the total device width and the initial state variable x_0 = (0.1 – 0.6), Ron = (100 – 1000 Ω), and r = (100 - 2000). In Fig. 34, a comparison is shown between the source voltage and the current flowing through the device as a function of time. It can be seen that, although the current shows a delay relative to the voltage, both curves have the same period, which demonstrates that the memristor does not store charge but is a purely dissipative device [65].

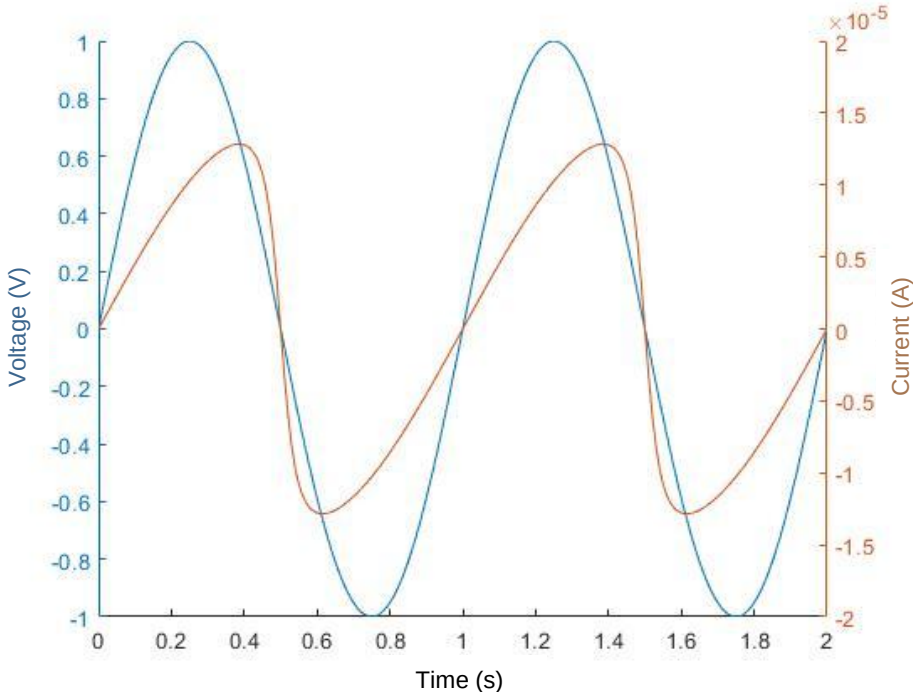

Fig. 34 | Voltage and Current curves as a function of time.

Changes in the state variable and the device's memristance as a function of time are shown in the Fig. 35a and Fig. 35b respectively, it can be observed that when the state variable W reaches its maximum value, the memristance is at its minimum and vice versa, this occurs because when the state variable value is at its maximum, the doped region is large, making the device more dielectric than metallic.

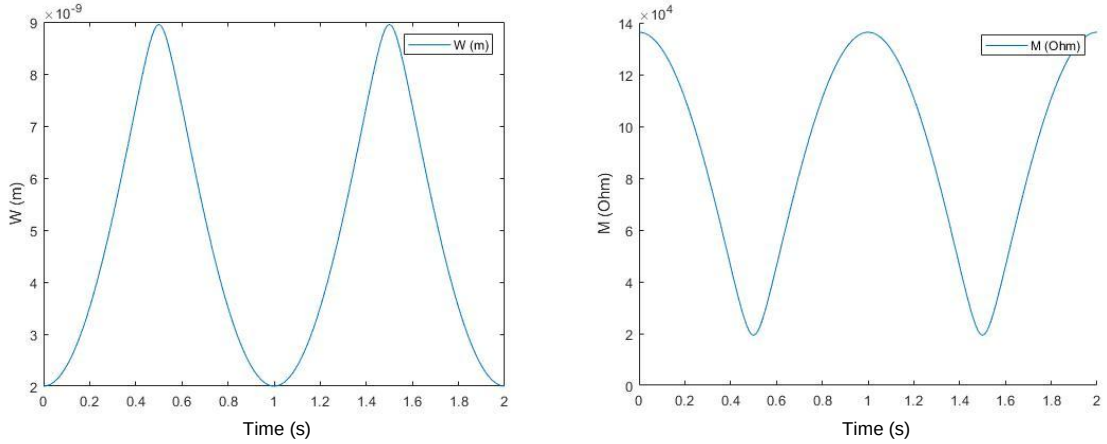

Fig. 35 | a) State variable "W" as a function of time, b) Memristance as a function of time.

Figure 36a shows the device's I-V curve, where a smooth and symmetrical hysteresis cycle characteristic of an ideal memristor is observed. This behavior represents how the current and voltage change through time. The smoothness of the cycle indicates that the memristor is operating in an ideal state without boundary drift resistance. The hysteresis cycle is a key characteristic of memristors that makes them suitable for applications, such as the design of neuromorphic computation hardware, and represents graphically the memory properties of memristors.

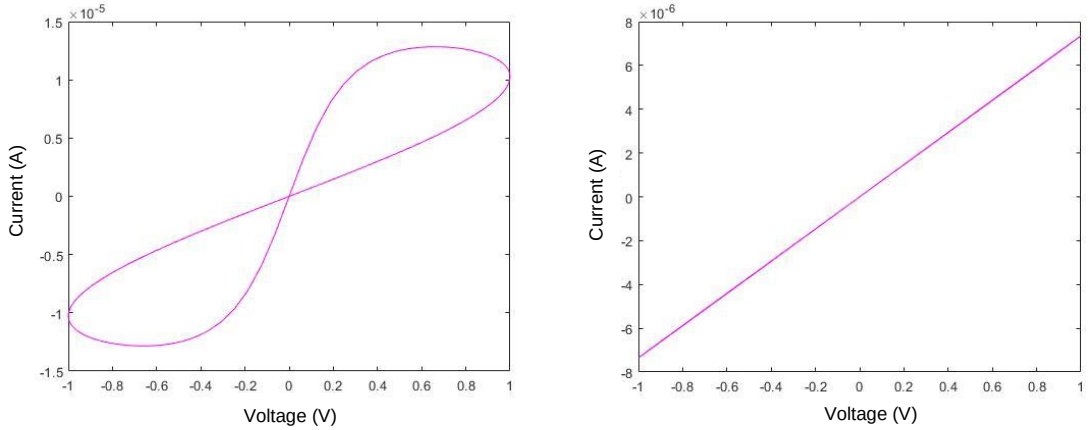

Fig. 36 | a) I-V curve of a memristor with 10 nm thickness, an ideal memristor behavior, b) I-V curve of a memristor with 100 nm thickness, hysteresis is lost, and the contact becomes ohmic.

A1.2.2 Nonlinear boundary drift models

The linear boundary drift model replicates the time-dependent hysteresis characteristic of memristor devices but oversimplifies fundamental electrodynamics. Specifically, even minimal voltages applied to nanometer-scale devices generate substantial electric fields, causing the ion boundary position to drift non-linearly. Moreover, the state variable W could never reach a zero length because this would mean no oxygen vacancies are present in the device, which is the identified charge transport mechanism. Furthermore, the full length of the device could become doped with oxygen vacancies. If we model the state change as a mass on a spring, the boundary drift velocity, v_D, should be highest at the device center and practically zero as W approaches either the edge W = 0 or W = D. These value restrictions for the boundary can be established by multiplying a window function to equation (15) as can be observed below [3], [65].

$$V_D = \frac{dw}{dt} = \frac{nu_D Ron}{D} i(t) F(x) \tag{27}$$

Where the normalized form of the state variable is given by x = W/D, the function F(x) attains its maximum value at the center of the device (x = 0.5) and approaches zero at the boundaries (x = 0 and x = 1). In the work of Joglekar et al. [3], [65], the following window function was proposed [65]

$$F_P(x) = 1 - (2x - 1)^{2p} \tag{28}$$

Where p is a positive integer. A graphical representation of the window function described in equation (28) for different p solutions (p = 1, 5, and 10) is presented in Fig. 37. The graph illustrates that the function reaches its maximum value at the center of the device and that at the boundaries the values are zero. Additionally, the rate of change of the function can be controlled by varying the parameter p. Lower values of p correspond to lower change rates, and vice versa. By substituting (28) into (27), we can obtain the modified state change equation:

$$\frac{dw}{dt} = \frac{nu_D Ron}{D} [1 - (2x - 1)^{2p}] \tag{29}$$

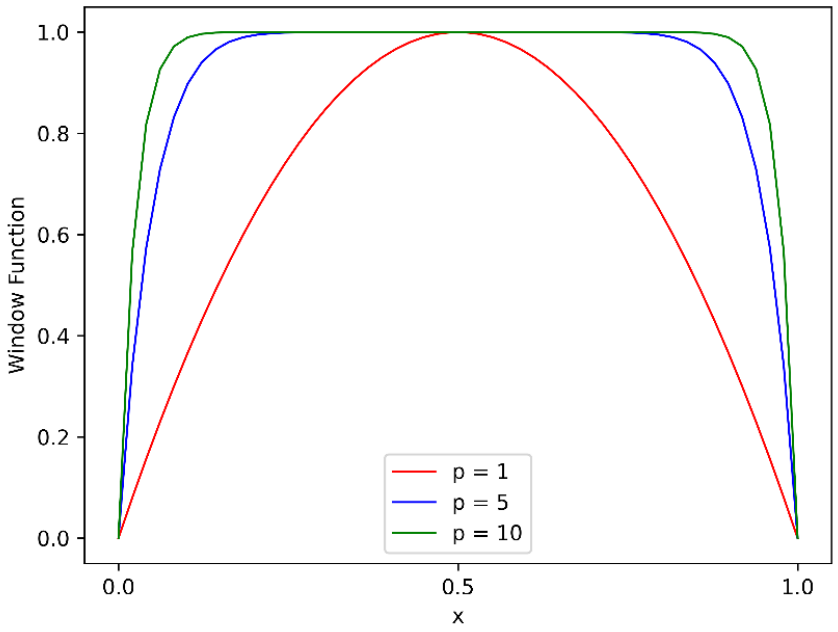

Fig. 37 | Plots of the non-linear window function proposed by Joglekar et al. for different p values [65].

As *p* increases, equation (29) approximates the linear boundary drift model defined in equation (15). This equation incorporates the *n* parameter to account for the inherent asymmetry of memristive devices. Maintaining a consistent specification of each device's physical orientation is essential during modeling and simulation. While the non-linear state change model in equation (29) offers a more precise physical representation than the linear model, the complexity introduced by the window function complicates the determination of the state variable W as a time-dependent function for arbitrary values of *p*. As a result, a time-step numerical solution method was adopted for simulations [65].

The equations delineated below were derived independently through systematic algebraic transformations of Equations (14), (19), and (29).

$$M(w) = Ron\left(\frac{w(t_i)}{D}\right) + Roff\left(1 - \frac{w(t_i)}{D}\right) \tag{30}$$

$$I(t_{i+1}) = \frac{v(t_{i+1})}{M\big(w(t_i)\big)} \tag{31}$$

$$V_D(t_{i+1}) = \frac{nu_D R_n}{D} I(t_{i+1}) F_p\left(\frac{w(t_i)}{D}\right) \tag{32}$$

$$w(t_{i+1}) = v_D(t_{i+1})[t_{i+1} - t_i] + w(t_i) \tag{33}$$

$$q(t_{i+I}) = \frac{\phi(t_{i+1})}{M\big(w(t_i)\big)} \tag{34}$$

Where t_i in equation (30) corresponds to the initial time step and t_{i+1} in equations (31) to (34), the following integral time step. The order of these time-step equations reveals an additional complication associated with the practical implementation of equation (28), particularly when the doped region fully extends across the entire length of the device (x = 1). According to Equation (28), $F_p(x = 1) = 0$ for every value of *p*. Consequently, as per Equation (32), with $V_D = 0$, the state variable *w* described in Equation (33) remains unaltered, ensuring that x retains a value of 1 in the subsequent simulation time-step. Subsequently, this loop stays active until the simulation concludes, regardless of any reversal in current polarity, thereby leading to erroneous results [65].

To address this problem, Biolek et al. proposed another window function [65], [67].

$$F_p(x) = 1 - [x - u(-I)]^{2p} \tag{35}$$

Where

$$u(I) = \begin{cases} 1, if\ I \geq 0 \\ 0, if\ I < 0 \end{cases} \tag{36}$$

Fig. 38 displays the window function for various values of p (*p* = 1, 5, and 10). In this formulation, the evolution of the state variable is no longer analogized to a mass-spring system. Instead, the window function exhibits asymmetry in regulating variations in V_D. For instance, starting from *x = 0*, the function has an initial value of 1. As *x* increases toward *D*, the function monotonically decreases toward 0. Upon the current direction reversal, the function instantaneously resets to 1. As *x* decreases back toward 0, the function decays to 0. The cycle repeats upon each reversal of current direction. Equation (35) can be directly substituted into equation (32) to evaluate V_D without modifying the remaining four governing equations. A key benefit of Biolek's proposed window function is its ability to prevent convergence problems at the device boundaries [65].

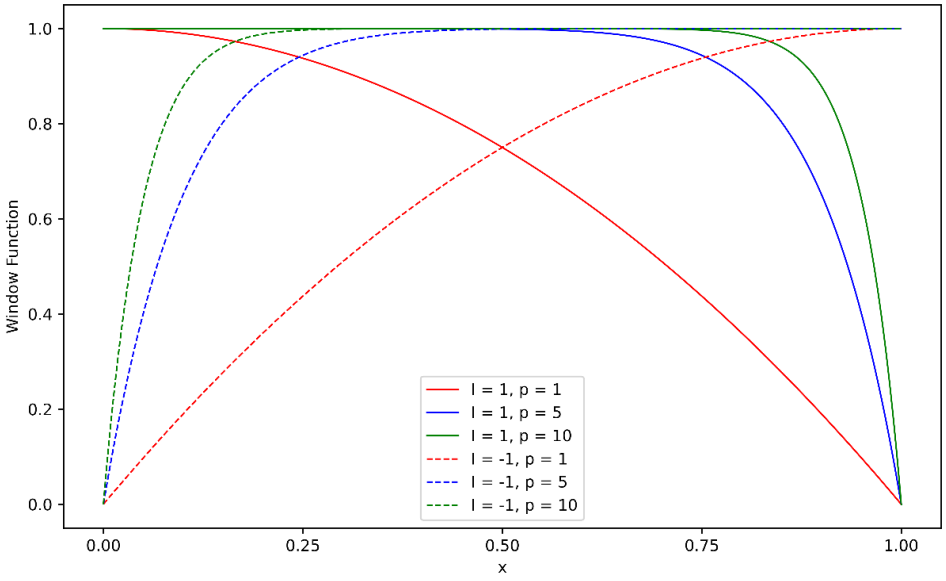

Fig. 38 | Plots of the non-linear window function proposed by Biolek et al. for different p values [65]**.**

For simulating and modeling the memristor nonlinear boundary drift model, the optimal time-step values, $\Delta t = t_{i+1} - t_i$, were determined to be between 10^{-2} and 10^{-4} seconds. The simulation results employing Joglekar's window function are presented in Fig. 39. Notably, the current-voltage characteristics displayed in Fig. 39a and Fig. 39c exhibit increased sharpness, directly attributed to the windowing mechanism that modulates the device's response. Additionally, while not graphically depicted, the data indicate that for high integer values of the exponent parameter *p*, the nonlinear model's response converges toward its linear counterpart. Furthermore, a detailed examination reveals that the temporal evolution of both memristance and the internal state variable *w* remains highly consistent across the linear and nonlinear configurations [65]. This convergence in the state dynamics suggests that the introduction of the window function significantly impacts the I-V transition characteristics, while essentially leaving the underlying state evolution mechanisms unchanged.

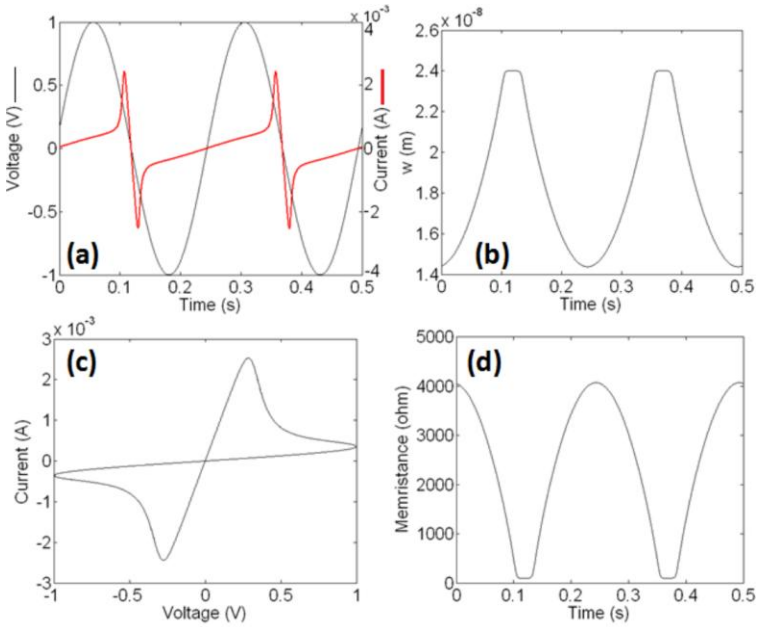

Fig. 39 | Plots of a) current and voltage as function of time, b) w(t), c) V-I hysteresis behavior, and d) M(t) memristor simulation results using non-linear dopant drift model and Joglekar's window function, with parameters $\mu D = 6.4 \times 10^{-14}$ $m^2V^{-1}s^{-1}$, D = 24 nm, $w_0/D = 0.6$, Ron = 100 Ω, r = 100, p = 7, $v_0 = 1$ V, $\omega = 8\pi$ rad/s, $V(t) = \sin(8\pi t + 0.16)$ V, $\Phi(t) = (1/8\pi)[\cos(0.16) - \cos(8\pi t + 0.16)]$ Wb, and $\Delta t = 10^{-4}$ sec [65].

The electrical response of memristive devices may exhibit transient variability over several cycles before stabilizing into a consistent behavioral pattern under specific parameter conditions. However, the initial variability can be mitigated by selecting an appropriate phase shift, as demonstrated in the results of Fig. 39, where a 0.16 rad phase shift was implemented. The window function enhances the model's robustness regarding the selection of arbitrary parameter ranges. Furthermore, the impact of parameter tuning and adjustment is comparable for both linear and nonlinear models. Regarding simulation stability, certain nonlinear models exhibit limitations in simulation duration when Joglekar's window function is employed, which prevents execution over arbitrary time spans. The convergence-related simulation failure can be partially mitigated by increasing the value of D (up to approximately 50 nm), while maintaining physically realistic device dimensions. However, this adjustment does not constitute a comprehensive solution. Biolek's window function can be used as an alternative to address the convergence issues inherent in Joglekar's window function. Simulation results obtained using this approach are presented in Fig. 40. The plots demonstrate that the model retains the highly nonlinear characteristics inherent to memristive device behavior. Furthermore, Biolek's window function introduces a distinct advantage by enabling the modeling of general asymmetric current-voltage (I–V) characteristics—capabilities that are largely unattainable using the two preceding models under typical operating conditions. This function is particularly noteworthy given that a substantial portion of

experimentally reported physical memristor data displays pronounced asymmetry in its I–V behavior [65].

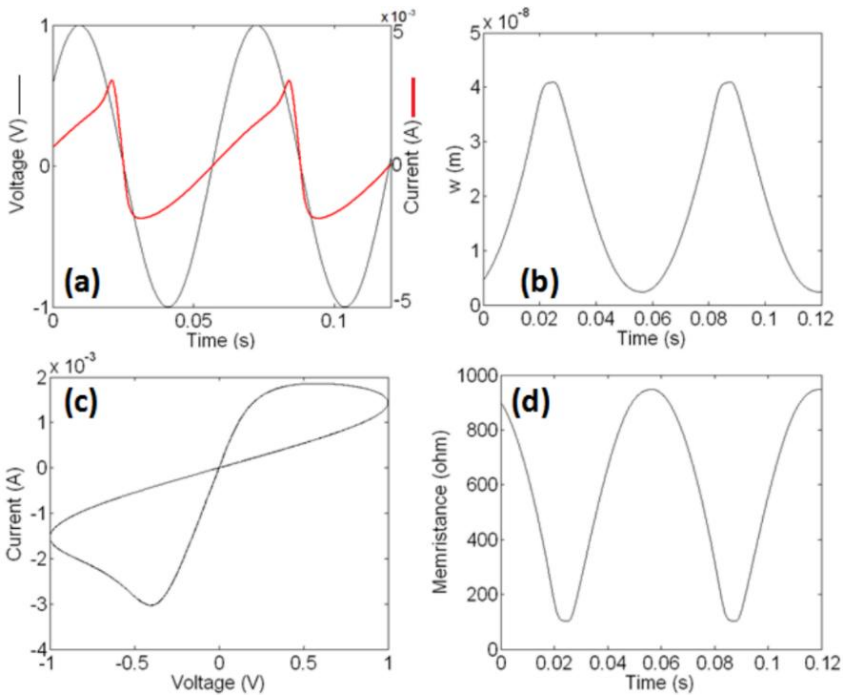

Fig. 40 | Plots of a) current and voltage as function of time, b) w(t), c) V-I hysteresis behavior, and d) M(t) memristor simulation results using non-linear dopant drift model and Biolek's window function, with parameters $\mu D = 4.4x10^{-13}$ $m^2V^{-1}s^{-1}$, D = 41 nm, $w_0/D = 0.11$, Ron = 100 Ω, r = 10, p = 7, $v_0 = 1$ V, ω = 100 rad/s, V(t) = sin(100 t + 0.62) V, Φ(t) = (0.01) [cos(0.62) – cos(100π t + 0.62)] Wb, and $\Delta t = 10^{-4}$ sec [65].

A1.3 Resistive switching behavior

As mentioned earlier, memristive devices exhibit changes in their resistance in response to specific electrical stimuli. In general, two distinct switching modes—unipolar (or nonpolar) and bipolar—are recognized in anionic and cationic memristive devices. Fig. 41 presents the I-V curve characteristics of unipolar and bipolar resistive switching. In the unipolar resistive switching shown in Fig. 41a, the resistive state change depends only on the magnitude of the applied voltage, while the polarity does not affect the resistance changes. The SET process—in which the device turns to an ON state (low resistance state)—occurs at a higher voltage than that required for the RESET operation—where the device turns to an OFF state (high resistance state)—additionally, the current level reached at the RESET transition point is greater than the compliance current defined during the SET operation. As observed in Fig. 41b, the bipolar mode relies on using opposite voltage polarities as a key requirement to switch the device ON and OFF, respectively.

Frequently, some asymmetry in the I-V curve characteristics can be observed in both switching modes, which can be tailored through device engineering or electrical forming [68].

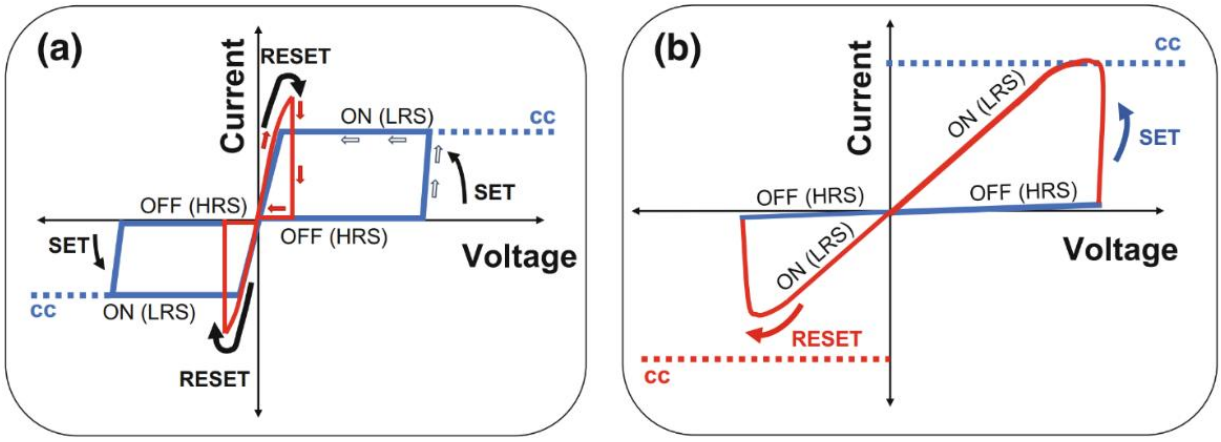

Fig. 41 | I-V curve switching characteristics of memristors a) unipolar switching b) bipolar switching, "compliance current = cc" [68].

Although resistive switching is electrically induced in both switching modes, the driving force is quite different, governed by the relative implications of the electric field and Joule heating in controlling the formation and stability of conductive channels. In a general sense, a memristor switching tends to be unipolar when Joule heating effects dominate and bipolar when electric field effects are mainly involved [68]. In memristive switching, the electric field and Joule heating are always present, but their influence differs based on factors such as the device structure, material composition, and past electrical activity. As a result, oxide-based switches typically exhibit four primary types of switching behavior: bipolar nonlinear, bipolar linear, nonpolar bistable, and nonpolar threshold switching. Schematics of the four types of switching are shown in Fig. 42a-d. In every instance, atomic motion or rearrangement is driven by four key forces that can act independently or in combination: the electric potential gradient (field), electron kinetic energy, species concentration gradient, and temperature gradient, as shown in Fig. 42e-h [69]. A strong electric field gradient can transport charged dopants, while high-velocity electrons in such a field can shift atoms through momentum transfer, a phenomenon known as "electron wind". This effect has been shown to enable reversible resistance switching in gold nanowires as presented in the work of S. L. Johnson et. al. [70].

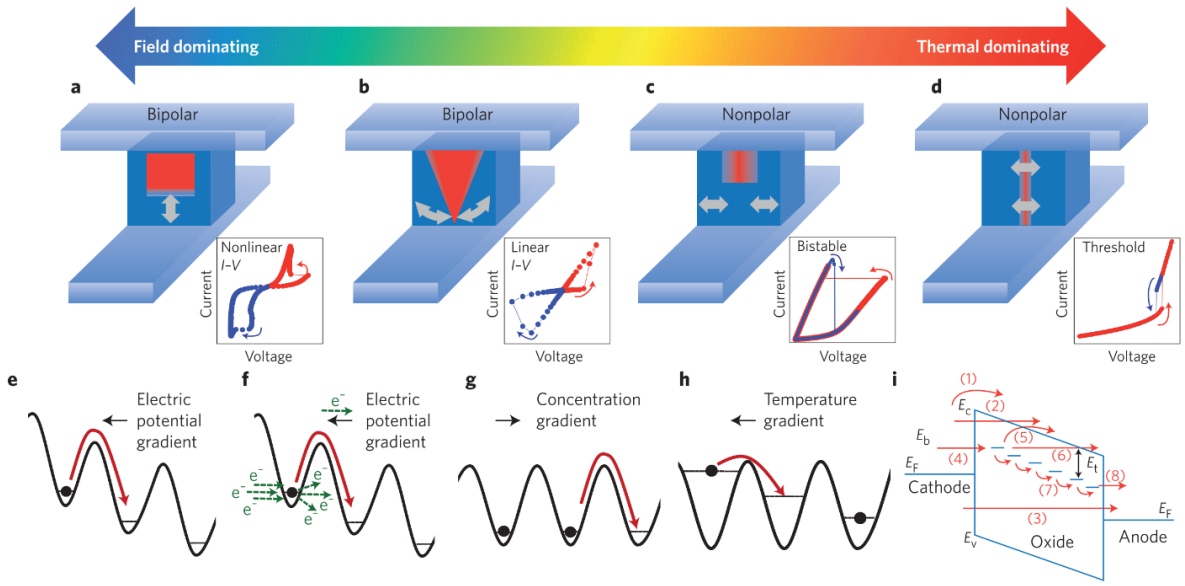

Fig. 42 | Schematics of the driving forces, electrical characteristics, transport mechanisms of ions and electrons for the switching of anion-based devices. a-d) Schematics of conductive channels in four switching devices, in which the electric field and Joule heating control the resistance switching. [69].

The electric field and electron kinetic energy are governed by polarity and can induce bipolar switching. In contrast, Joule heating plays a more complex role that remains only partially understood. However, the high temperatures it generates greatly amplify both drift (Fig. 42e) and diffusion (Fig. 42g). Additionally, high temperatures are localized around the conductive channel, resulting in a high temperature gradient laterally. Analogous to an electric potential gradient or an element concentration gradient, a high temperature gradient can act as a driving force for a net mass transfer of atoms (Fig.42h). Drift and electromigration transport dopants vertically along the conduction channel, while the temperature gradient may facilitate their lateral movement. Diffusion occurs in both directions due to element concentration gradients present within the channel (vertically) and extending into and out of it (laterally). Ultimately, for each microscopic device state—defined by a specific distribution of impurities, defects, or dopants—the I–V characteristics are governed by the available electron conduction mechanisms, as illustrated in Fig. 42i for n-type materials [69]. An electric field driven device can be observed in Fig. 42a, the growth and retraction of the conduction channel under the electric field in the interface region results in the typical hysteresis switching loop, where the rectifying I-V curve in the OFF state and the symmetric nonlinear I-V curve in the ON state reflect a Schottky-like barrier and a residual tunnel barrier in the OFF and ON states, respectively. Figure 42b illustrates a different type of bipolar switching, where the I-V curve is linear in both the ON and OFF resistive states. This switching type involves a conduction channel continuously connecting the top and bottom electrodes throughout the switching cycle.

The resistance switching is driven by modifications in the composition, volume, or geometry within the conductive channel, influenced by a combination of electric-field-induced vertical drift and thermally enhanced lateral diffusion. As the thermal effect becomes more dominant, nonpolar switching emerges, allowing the same voltage polarity to both activate and deactivate the device, as shown in Fig. 42c. The underlying physics of this process remains a topic of debate. One perspective suggests that the temperature gradient depicted in Fig. 42h could facilitate the migration of oxygen vacancies toward the conduction channel, effectively turning the device to the ON state. Conversely, the set switching initially behaves like a "soft breakdown" of dielectrics under an applied electric field. It is likely a two-step process, where an initial electronic breakdown generates a high current, followed by heat-assisted ionic movement. In unipolar devices, the reset switching is typically characterized as a thermal rupture of the conduction channel, likely due to thermal diffusion driven by the concentration gradient, a reduction in the filament's free surface energy, or even a phase-change process induced by heat and/or an electric field.

On the other hand, the "threshold switching" shown in Fig. 42d is a volatile type of switching with a hysteresis loop. As the current increases, the insulating device suddenly transitions to a conductive state at a specific current threshold, resulting in a sharp increase in current on the I-V curve. Nevertheless, the device reverts to its insulating state after the current level is reduced. Consequently, this type of resistance switching is characterized as a purely thermally driven phenomenon [69].

A1.3.1 Unipolar switching

A tenable interpretation of unipolar switching behavior in metal-oxide-metal memristors involves a fuse-antifuse process governed by a filamentary conduction model [68]. This switching type is primarily driven by Joule heating, which induces localized thermal energy, facilitating mass transport and structural reconfiguration within the device [71]. According to this framework, the SET operation is achieved by thermally induced formation of nanoscale conductive filaments that span the entire oxide layer, while the RESET operation results from their subsequent rupture. In unipolar anionic devices, the initiation of these conductive filaments is primarily attributed to a pronounced temperature gradient within the device at the threshold SET or forming voltage, which drives thermophoretic effects and/or oxygen ion diffusion within the insulating layer [68], [72].

A1.3.2 Bipolar switching

Bipolar resistive switching is a polarity-dependent phenomenon in resistive memory devices, characterized by transitions between a high-resistance state (HRS) and a low-resistance state (LRS) under opposite voltage polarities. The 'set' operation (HRS to LRS) typically occurs when a positive bias is applied, while the 'reset' operation (LRS to HRS) requires a negative bias, or vice versa, depending on the device structure. This switching behavior arises from field-driven migration of defects, such as oxygen vacancies, resulting in the formation and rupture of conductive filaments or modulation of a tunneling barrier. In modeling contexts, accurately capturing this bipolar behavior requires the use of window functions and state-variable dynamics that reflect the asymmetric and nonlinear nature of the switching process.

This type of switching is predominantly exhibited in the majority of metal-oxide-based cationic devices as well as analogous anionic systems. The electrochemical metallization (ECM) mechanism can describe this characteristic polarity-dependent behavior. During the SET process, applying a positive bias to the active electrode facilitates the release of metal cations, which subsequently migrate through the solid electrolyte and undergo reduction at the inert counter electrode, forming conductive metallic filaments. The RESET transition is initiated by reversing the polarity, which induces the oxidative dissolution of these filaments at the active electrode, progressively disrupting the filamentary pathways and restoring the device to a high-resistance state. This reversible filament formation and rupture under opposing polarities underpin the bipolar switching behavior observed in such memristive systems [68].

A1.4 Resistive switching mechanisms

Resistive switching mechanisms describe the fundamental physical and chemical processes that enable a material to transition between distinct resistive states in response to an applied electric field. A precise evaluation is necessary to accurately determine the active material and switching mechanism, considering the potential chemical interactions that may occur within a device under the stress of an electric field and Joule heating. It is essential to consider the entire device stack of materials when analyzing memristors, as even the substrate material or electrodes can alter the device's switching behavior. It is common for the insulating material to undergo a phase transition during the initial electroforming or device fabrication stages, forming a novel phase responsible for the switching behavior. Consequently, accurately identifying the actual switching material is a challenging yet essential first step toward comprehending the underlying switching mechanism [69].

Memristive devices are required to exhibit a continuum of internal resistance states that can be adjusted in a quasi-stable fashion. The instantaneous resistive state is influenced by several critical parameters, notably externally controllable variables such as the applied electric field and compliance current during device characterization. Additionally, secondary synergistic factors — namely, electron mobility, gradients in species concentration, and temperature gradients within the insulating layer— are intrinsically linked to the semiconductor's solid-state properties, such as lattice defects. Consequently, fine-tuning these parameters often necessitates modifications to the fabrication process to achieve the desired device performance. The predominant model for resistive switching in metal-oxide memristors posits that reversible transitions between the HRS and LRS are mediated by the [68].

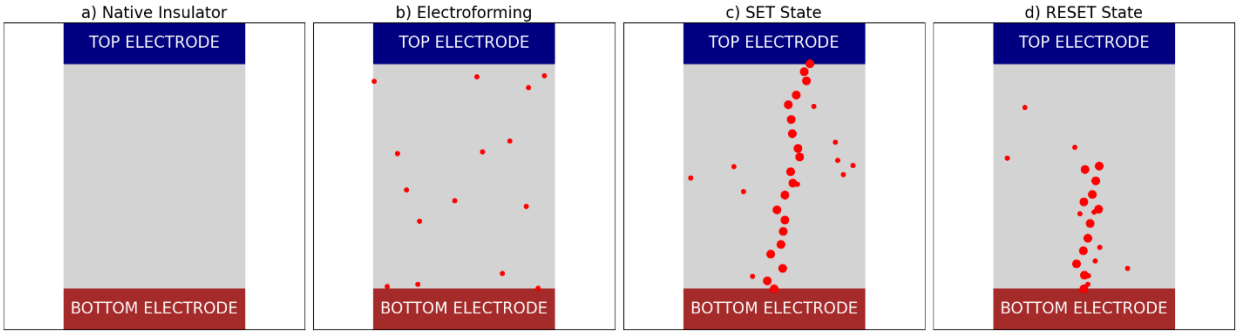

Fig. 43 | Filamentary conduction model schematic visualization of the resistive switching process. a) pristine insulator (HRS); b) electroforming of conductive channels; c) formation of conductive filaments in a SET process (ON state, causing the transition from HRS to LRS); d) rupture of the conductive filament in a RESET process (OFF state, representing the transition from LRS to HRS).

The formation of one or more filaments between the two electrodes induces the device to an LRS. In contrast, the rupture of the conductive filaments switches the device to an HRS, as shown in Fig. 43. According to the literature, the primary explanations for this model generally revolve around two key resistive switching mechanisms: the valence change mechanism (VCM) and the electrochemical metallization mechanism (ECM), both of which involve ion migration within the material. The valence change mechanism particularly builds on induced anion migration that progressively modifies the stoichiometry of the insulator region via oxidation-reduction reactions. The electrochemical metallization mechanism involves the oxidative dissolution of the active metal electrode at the interface, initiating the migration of cations through an ion-conducting electrolyte layer that functions as an insulator. An additional thermochemical process is considered in particular scenarios, complementing the primary mechanisms to explain structural and stoichiometric modifications in the insulating layer due to thermally induced effects from electrical current [68].

A1.5 Effects of electrode materials in memristive devices

The choice of electrode materials plays a critical role in the resistive switching properties of memristive devices. Chemical interactions at the electrode-active layer interface—such as vacancy migration, cation interdiffusion, and phase instability—can significantly affect device performance. Therefore, these interactions must be rigorously evaluated during the electrode selection process. The long-term operational behavior of the device is primarily determined by secondary interfacial interactions, which are influenced mainly by the electrode's work function—representing its electron-removal ionization energy—and the structural compatibility with the insulating layer's sublattice. This compatibility is determined by factors such as elemental size and crystal phase, which affect stability and performance over extended periods of use [68]. The assessment of the work function must be approached with caution, as it is highly dependent on crystallographic orientation, which directly influences measurement methodologies for pure electrode materials. Additionally, the local composition at the contact interface—shaped by the electrode deposition process and interfacial interactions within the MIM structure—can significantly modify the effective work function, impacting overall device performance.

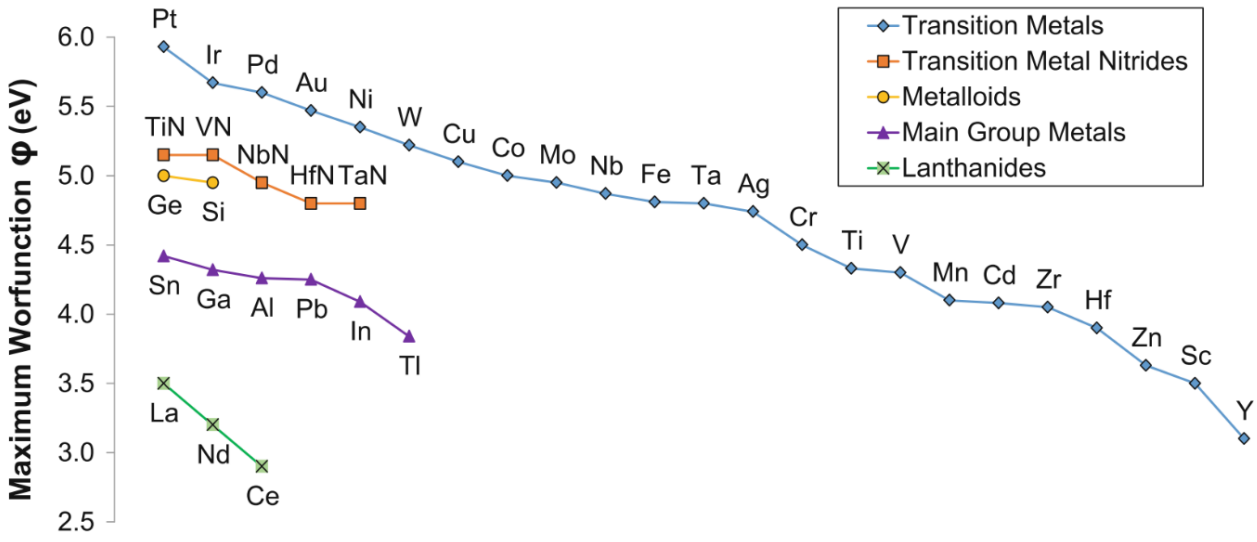

Fig. 44 | Work function of different semiconductor and metal elements [68].

A1.6 Active layer materials influence in memristive devices

The active layer materials have a significant impact on the resistive switching properties of a memristor; hence, choosing a suitable active material is an essential aspect of fabricating memristive devices. Several factors, such as the semiconducting properties and the Joule heating effects, play a key role in the design of functional MIM structures. A memristor requires an active layer with insulating and conductive properties to achieve resistive switching characteristics. In the literature have been established practices that ensure the formation and rupture of conductive filaments in semiconducting metal-oxide devices—such as (i) utilizing non-stoichiometric active materials, (ii) doping the insulator layer with one or more metal or metal-oxide, and (iii) making multilayered structures interfacing the insulating layer with a buffering agent lager—as can be seen in Fig. 45. There are different categories of active materials based on their anionic composition, crystal structure, dimensionality and films but more remarkably according to their unipolar and bipolar switching behavior. Metal-oxide-based insulators have received particular attention due to their simple atomic structure, good thermal stability, compatibility with CMOS technologies, and optimal switching characteristics [68].

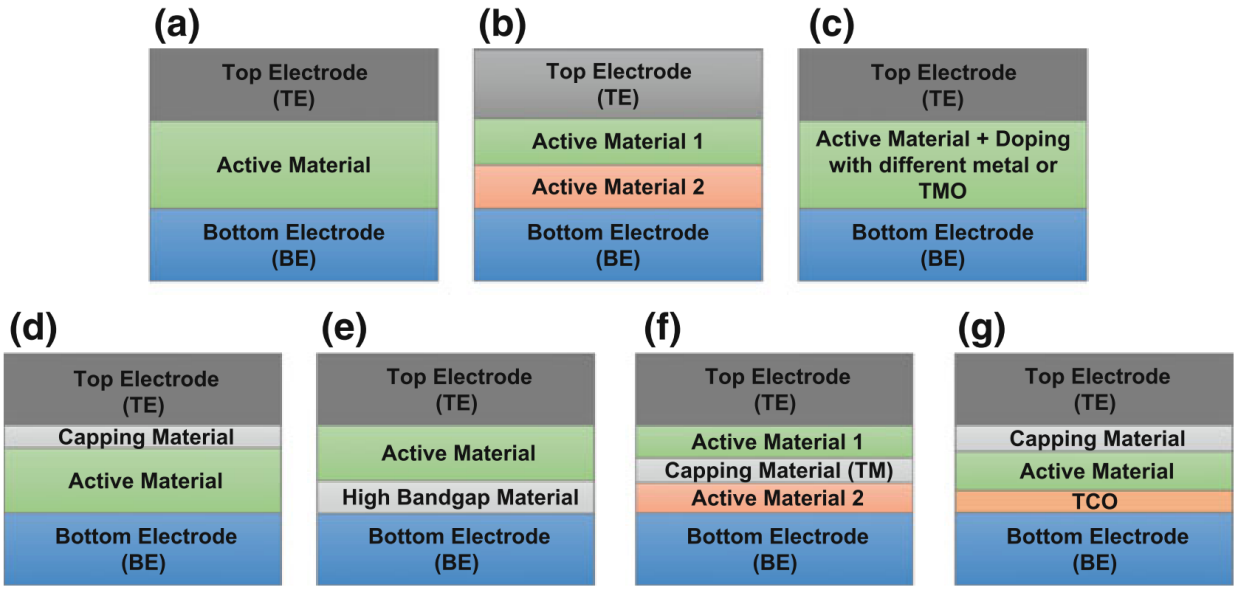

Fig. 45 | Schematic representation of MIM stacks reported in metal-oxide memristor literature. a) memristor device structure with just one layer of active material b) memristor device structure with a bilayer of active materials c) memristor device structure with the active material layer doped with a different metal d) memristor device structure with a bilayer conformed by active material and capping material layers e) memristor device structure with a bilayer conformed by active material and high bandgap material layers f) memristor device structure with a trilayer conformed by two active materials layers with a capping material layer in between g) memristor device structure with a trilayer conformed by a capping material layer, an active material layer and a TCO layer [68].

A1.7 Potential of memristors to emulate the biological synapse

Memristors have garnered significant attention as artificial synaptic elements in neuromorphic engineering due to their inherent ability to exhibit analog, history-dependent conductance changes. These devices naturally emulate synaptic plasticity mechanisms such as long-term potentiation (LTP), long-term depression (LTD), and spike-timing-dependent plasticity (STDP), enabling their use in neuromorphic computational systems. The modulation of conductance in memristive devices, governed by the time and polarity of electrical pulses, mirrors the weight adaptation observed in biological synapses, allowing for direct hardware implementation of learning rules in spiking neural networks [69], [73]. Several key metrics are assessed to evaluate the suitability of memristors as synaptic mimics, including conductance dynamic range, symmetry and linearity of potentiation/depression cycles, retention time, switching energy, and endurance. Pulse-train protocols are commonly used to characterize incremental conductance changes and to simulate synaptic learning behaviors [74]. Given their nanoscale scalability, low power consumption, and compatibility with CMOS processes, memristors offer a promising pathway toward scalable, energy-efficient neuromorphic architectures [75].

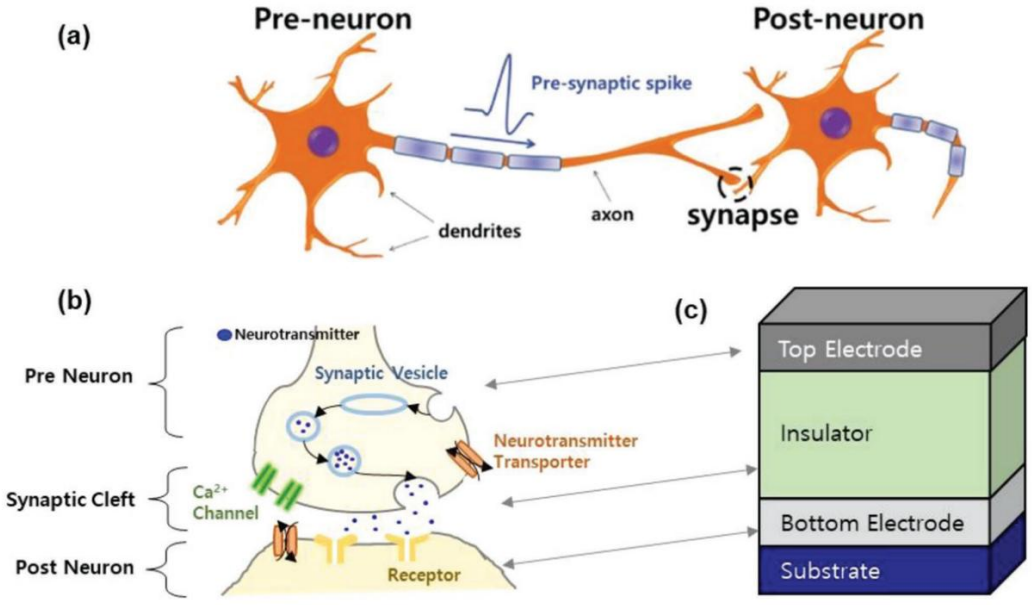

Fig. 46 | a) Schematic diagram of a presynaptic neuron, a postsynaptic neuron and the synapse, b) schematic diagram of the neurotransmission process, c) general structure of the memristor-based synapse [76]**.**

A1.7.1 Synaptic plasticity mechanisms in memristors

Biological synapses adapt their strength in response to neural activity, enabling learning and memory processes. This adaptive capability, known as synaptic plasticity, is primarily governed by mechanisms such as LTP, LTD and STDP. Due to their nonlinear and history-dependent conductance modulation, memristors are capable of emulating these behaviors in hardware. The subsections below describe each plasticity mechanism and the methods commonly used to evaluate their analogs in memristive devices.

A1.7.2 Long-term potentiation (LTP)

Long-term potentiation is the process by which synaptic strength increases due to repeated and sustained pre-synaptic stimulation. In biological systems, this strengthens the connection between neurons and is associated with the process of learning. In memristors, LTP is emulated by applying a train of pulses of one polarity (depending on the device materials) that gradually reduce the device resistance, increasing the conductance state. This gradual modification corresponds to a transition toward an LRS.

Evaluation in Memristors

- **A series of identical voltage pulses (SET pulses that stimulate a conductance increase) is applied with fixed intervals.**
- **After each pulse or every few pulses, the read conductance is measured at a small, non-disturbing voltage (this voltage usually has a smaller amplitude than the SET pulse to ensure that the device's state remains unaltered).**
- **The conductance vs pulse number is plotted to observe the potentiation trend.**
- **Ideal LTP emulation exhibits a gradual, monotonic increase in conductance, characterized by good linearity and repeatability.**

A1.7.3 Long-term depression (LTD)

Long-term depression is the opposite of LTP and represents a decrease in synaptic strength due to specific patterns of activity or a lack of stimulation associated with forgetting. It is essential for synaptic weight balancing and memory erasure. In memristors, this is typically achieved by applying a train of pulses with the opposite polarity from LTP, depending on the device materials, which increases the device resistance and decreases its conductivity.

Evaluation in Memristors

- **Similar to LTP testing, but with a stimulus of pulses that cause a reduction in conductance.**
- **A read pulse that doesn't alter the device state is used to measure the device conductance and observe the depression behavior.**
- **Ideally, LTD shows a gradual decrease in conductance that is symmetric and consistent with LTP behavior.**

A1.7.4 Spike-timing-dependent plasticity (STDP)

The STDP is a biologically realistic rule where the change in synaptic weight depends on the relative timing between pre-synaptic and post-synaptic spikes. If the pre-synaptic neuron fires shortly before the post-synaptic one ($\Delta t > 0$), LTP occurs; if it fires after ($\Delta t < 0$), LTD occurs. To emulate STDP in memristors, overlapping bipolar pulse pairs are used to simulate the timing of pre-and post-synaptic spikes. The overlap (Δt) of these pulses determines the net voltage across the device and, therefore, the direction and magnitude of the conductance change.

Evaluation in Memristors:

- **Pre- and post-synaptic pulses are generated with variable time delays.**
- **The change in conductance (ΔG) is measured after each pulse pair.**
- **A ΔG vs. Δt plot is generated, which ideally resembles the exponential STDP learning window observed in biological systems:**

$$\Delta G(\Delta t) \propto \begin{cases} +A_{+}e^{\left(\frac{-\Delta t}{\tau_{+}}\right)}, \text{if} \Delta t > 0 \\ -A_{-}e^{\left(\frac{\Delta t}{\tau_{-}}\right)}, \text{if} \Delta t < 0 \end{cases} \quad (37)$$

REFERENCES

[1] M. Ismail, M. Rasheed, C. Mahata, M. Kang, and S. Kim, “Nano-crystalline ZnO memristor for neuromorphic computing: Resistive switching and conductance modulation,” *J Alloys Compd*, vol. 960, Oct. 2023, doi: 10.1016/j.jallcom.2023.170846.

[2] L. 0 Chua, “Memristor-The Missing Circuit Element,” Sep. 1971. doi: https://doi.org/10.1109/TCT.1971.1083337.

[3] Y. N. Joglekar and S. J. Wolf, “The elusive memristor: properties of basic electrical circuits,” *Eur J Phys*, vol. 30, no. 4, pp. 661–675, Jul. 2009, doi: 10.1088/0143-0807/30/4/001.

[4] S. Askaruly and B. Rakhmetov, “The Representation of Memristor Model in MATLAB® and Simulink® Environment,” Research Publishing Services, Jun. 2015, pp. 76–79. doi: 10.3850/978-981-09-4424-7_82.

[5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[6] J. L. Vazquez-Arce, J. Molina-Reyes, O. E. Contreras, and H. Tiznado, “A Voltage-Driven Transport Model to Identify Ion Migration as the Rate-Limiting Step in Memristive Switching,” *Adv Electron Mater*, vol. 10, no. 1, Jan. 2024, doi: 10.1002/aelm.202300608.

[7] Y. Xiao *et al.*, “A review of memristor: material and structure design, device performance, applications and prospects,” 2023, *Taylor and Francis Ltd.* doi: 10.1080/14686996.2022.2162323.

[8] C. Mahata, J. Park, M. Ismail, D. H. Kim, and S. Kim, “Improved Resistive Switching with Low-Power Synaptic Behaviors of ZnO/Al2O3 Bilayer Structure,” *Materials*, vol. 15, no. 19, Oct. 2022, doi: 10.3390/ma15196663.

[9] T. Cheng, J. Rao, X. Tang, L. Yang, and N. Liu, “Analog memristive characteristics and conditioned reflex study based on Au/ZnO/ITO devices,” *Electronics (Switzerland)*, vol. 7, no. 8, Aug. 2018, doi: 10.3390/electronics7080141.

[10] K. Bejtka, G. Milano, C. Ricciardi, C. F. Pirri, and S. Porro, “TEM Nanostructural Investigation of Ag-Conductive Filaments in Polycrystalline ZnO-Based Resistive Switching Devices,” *ACS Appl Mater Interfaces*, vol. 12, no. 26, pp. 29451–29460, Jul. 2020, doi: 10.1021/acsami.0c05038.

[11] C. Hao, J. Peng, R. Zierold, and R. H. Blick, “Atomic Layer Deposition Films for Resistive Random-Access Memories,” Aug. 21, 2024, *John Wiley and Sons Inc*. doi: 10.1002/admt.202301762.

[12] L. G. Wang *et al.*, “Excellent resistive switching properties of atomic layer-deposited Al2O3/HfO2/Al2O3 trilayer structures for non-volatile memory applications,” *Nanoscale Res Lett*, vol. 10, no. 1, Dec. 2015, doi: 10.1186/s11671-015-0846-y.

[13] M. Trapatseli, S. Cortese, A. Serb, A. Khiat, and T. Prodromakis, “Impact of ultra-thin Al2O3-y layers on TiO2-x ReRAM switching characteristics,” *J Appl Phys*, vol. 121, no. 18, May 2017, doi: 10.1063/1.4983006.

[14] C. F. Chiu, S. Ginnaram, A. Senapati, Y. P. Chen, and S. Maikap, “Switching characteristics and mechanism using Al2O3 interfacial layer in Al/Cu/GdOx/Al2O3/Tin memristor,” *Electronics (Switzerland)*, vol. 9, no. 9, pp. 1–16, Sep. 2020, doi: 10.3390/electronics9091466.

[15] “Sung Il Park thesis for esubmission with title page-augmented”, Accessed: Sep. 25, 2025. [Online]. Available: http://purl.stanford.edu/cs381qx1114

[16] Z. Jie Tan, V. Somjit, C. Toparli, B. Yildiz, and N. Fang, “Electronegative metal dopants improve switching consistency in Al 2 O 3 resistive switching devices.”

[17] R. Waser and M. Aono, “Nanoionics-based resistive switching memories,” 2007. [Online]. Available: www.nature.com/naturematerials

[18] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, “Memristive switching mechanism for metal/oxide/metal nanodevices,” *Nat Nanotechnol*, vol. 3, no. 7, pp. 429–433, 2008, doi: 10.1038/nnano.2008.160.

[19] M. J. Lee *et al.*, “A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5-xx/TaO2-xbilayer structures,” *Nat Mater*, vol. 10, no. 8, pp. 625–630, 2011, doi: 10.1038/nmat3070.

[20] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, “Erratum: Electrochemical metallization memories - Fundamentals, applications, prospects (Nanotechnology (2011) 22 (254003)),” Jul. 15, 2011. doi: 10.1088/0957-4484/22/28/289502.

[21] A. Kumar and M. S. Baghini, “Experimental study for selection of electrode material for ZnO-based memristors,” *Electron Lett*, vol. 50, no. 21, pp. 1547–1549, Oct. 2014, doi: 10.1049/el.2014.1491.

[22] D. H. Kwon *et al.*, “Atomic structure of conducting nanofilaments in TiO2 resistive switching memory,” *Nat Nanotechnol*, vol. 5, no. 2, pp. 148–153, 2010, doi: 10.1038/nnano.2009.456.

[23] A. Prakash, D. Jana, and S. Maikap, “TaOx-based resistive switching memories: Prospective and challenges,” 2013, *Springer New York LLC*. doi: 10.1186/1556-276X-8-418.

[24] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[25] A. Sawa, “Resistive switching in transition metal oxides,” Elsevier, Jun. 2008. doi: https://doi.org/10.1016/S1369-7021(08)70119-6.

[26] H. S. P. Wong *et al.*, “Metal-oxide RRAM,” in *Proceedings of the IEEE*, Institute of Electrical and Electronics Engineers Inc., 2012, pp. 1951–1970. doi: 10.1109/JPROC.2012.2190369.

[27] D. Ielmini and H. S. P. Wong, “In-memory computing with resistive switching devices,” Jun. 01, 2018, *Nature Publishing Group*. doi: 10.1038/s41928-018-0092-2.

[28] M. Seal, A. Deogaonkar, A. Senapati, S. Maikap, and N. Raghavan, “Ruthenium based RRAM for low variability switching and scaling for contemporary computing systems,” *Microelectronics Reliability*, vol. 138, Nov. 2022, doi: 10.1016/j.microrel.2022.114623.

[29] J. H. Yoon *et al.*, “A Low-Current and Analog Memristor with Ru as Mobile Species,” *Advanced Materials*, vol. 32, no. 9, Mar. 2020, doi: 10.1002/adma.201904599.

[30] J. E. Kim *et al.*, “Low Energy and Analog Memristor Enabled by Regulation of Ru ion Motion for High Precision Neuromorphic Computing,” *Adv Electron Mater*, vol. 8, no. 10, Oct. 2022, doi: 10.1002/aelm.202200365.

[31] Y. Feng *et al.*, “Negative Differential Resistance Effect in Ru-Based RRAM Device Fabricated by Atomic Layer Deposition,” *Nanoscale Res Lett*, vol. 14, 2019, doi: 10.1186/s11671-019-2885-2.

[32] M. Ismail *et al.*, “Enhanced analog switching and neuromorphic performance of ZnO-based memristors with indium tin oxide electrodes for high-accuracy pattern recognition,” *Journal of Chemical Physics*, vol. 161, no. 13, Oct. 2024, doi: 10.1063/5.0233031.

[33] F. Wu and T. Y. Tseng, “All-Optically Regulated ITO/Cu2O/WO3/ITO Memristor for Optoelectronic Neuromorphic Computing,” *ACS Appl Electron Mater*, vol. 6, no. 7, pp. 5212–5221, Jul. 2024, doi: 10.1021/acsaelm.4c00726.

[34] B. Jeon and S. Kim, “Effect of ITO electrode on conductance quantization and multi-level cells in TiN/SiOx/ITO devices,” *Ceram Int*, vol. 49, no. 1, pp. 425–430, Jan. 2023, doi: 10.1016/j.ceramint.2022.09.007.

[35] Q. Qiao, D. Xu, Y. W. Li, J. Z. Zhang, Z. G. Hu, and J. H. Chu, “Detection of resistive switching behavior based on the Al2O3/ZnO/Al2O3 structure with alumina buffers,” *Thin Solid Films*, vol. 623, pp. 8–13, Feb. 2017, doi: 10.1016/j.tsf.2016.12.053.

[36] H. Guo *et al.*, “Enhancing Resistive Switching in AlN-Based Memristors Through Oxidative Al2O3 Layer Formation: A Study on Preparation Techniques and Performance Impact,” *Micromachines (Basel)*, vol. 15, no. 12, Dec. 2024, doi: 10.3390/mi15121499.

[37] Z. Yu *et al.*, “Tunable Resistive Switching Behaviors and Mechanism of the W/ZnO/ITO Memory Cell,” *Molecules*, vol. 28, no. 14, Jul. 2023, doi: 10.3390/molecules28145313.

[38] Y. J. An *et al.*, “Effects of thermal annealing on analog resistive switching behavior in bilayer HfO2/ZnO synaptic devices: the role of ZnO grain boundaries,” *Nanoscale*, vol. 16, no. 9, pp. 4609–4619, Jan. 2024, doi: 10.1039/d3nr04917e.

[39] T. Sun *et al.*, “Stable Resistive Switching in ZnO/PVA:MoS2 Bilayer Memristor,” *Nanomaterials*, vol. 12, no. 12, Jun. 2022, doi: 10.3390/nano12121977.

[40] M. Lanza *et al.*, “Recommended Methods to Study Resistive Switching Devices,” Jan. 01, 2019, *Blackwell Publishing Ltd*. doi: 10.1002/aelm.201800143.

[41] M. Lanza *et al.*, “Standards for the Characterization of Endurance in Resistive Switching Devices,” Nov. 23, 2021, *American Chemical Society*. doi: 10.1021/acsnano.1c06980.

[42] F. J. Alonso, D. Maldonado, A. M. Aguilera, and J. B. Roldán, “Memristor variability and stochastic physical properties modeling from a multivariate time series approach,” *Chaos Solitons Fractals*, vol. 143, Feb. 2021, doi: 10.1016/j.chaos.2020.110461.

[43] X. Lian *et al.*, “Resistance switching statistics and mechanisms of Pt dispersed silicon oxide-based memristors,” *Micromachines (Basel)*, vol. 10, no. 6, Jun. 2019, doi: 10.3390/mi10060369.

[44] D. S. Woo *et al.*, “Unveiling the Resistive Switching Mechanism and Low Current Dynamics of Ru-based Hybrid Synaptic Memristors,” *Adv Funct Mater*, vol. 35, no. 9, Feb. 2025, doi: 10.1002/adfm.202416309.

[45] A. V. Saenko *et al.*, “Transparent Zinc Oxide Memristor Structures: Magnetron Sputtering of Thin Films, Resistive Switching Investigation, and Crossbar Array Fabrication,” *Nanomaterials*, vol. 14, no. 23, Dec. 2024, doi: 10.3390/nano14231901.

[46] F. M. Simanjuntak, D. Panda, K. H. Wei, and T. Y. Tseng, “Status and Prospects of ZnO-Based Resistive Switching Memory Devices,” Dec. 01, 2016, *Springer New York LLC*. doi: 10.1186/s11671-016-1570-y.

[47] W. H. Xue *et al.*, “Intrinsic and interfacial effect of electrode metals on the resistive switching behaviors of zinc oxide films,” *Nanotechnology*, vol. 25, no. 42, Oct. 2014, doi: 10.1088/0957-4484/25/42/425204.

[48] J. Molina *et al.*, “Influence of the surface roughness of the bottom electrode on the resistive-switching characteristics of Al/Al2O3/Al and Al/Al2O3/W structures fabricated on glass at 300 °c,” *Microelectronics Reliability*, vol. 54, no. 12, pp. 2747–2753, Dec. 2014, doi: 10.1016/j.microrel.2014.07.006.

[49] V. Yon, A. Amirsoleimani, F. Alibart, R. G. Melko, D. Drouin, and Y. Beilliard, “Exploiting Non-idealities of Resistive Switching Memories for Efficient Machine Learning,” *Frontiers in Electronics*, vol. 3, Mar. 2022, doi: 10.3389/felec.2022.825077.

[50] J. Heo, S. Kim, S. Kim, and M. H. Kim, “Configurable Synaptic and Stochastic Neuronal Functions in ZnTe-Based Memristor for an RBM Neural Network,” *Advanced Science*, vol. 11, no. 42, Nov. 2024, doi: 10.1002/advs.202405768.

[51] H. W. Choi *et al.*, “Zinc oxide and indium-gallium-zinc-oxide bi-layer synaptic device with highly linear long-term potentiation and depression characteristics,” *Sci Rep*, vol. 12, no. 1, Dec. 2022, doi: 10.1038/s41598-022-05150-w.

[52] S. Park, B. Spetzler, T. Ivanov, and M. Ziegler, “Multilayer redox-based HfOx/Al2O3/TiO2 memristive structures for neuromorphic computing,” *Sci Rep*, vol. 12, no. 1, Dec. 2022, doi: 10.1038/s41598-022-22907-5.

[53] P. Dacha *et al.*, “Solution Shearing of Sustainable Aluminum Oxide Thin Films for Compliance-Free, Voltage-Regulated Multi-Bit Memristors,” *Adv Electron Mater*, vol. 11, no. 7, May 2025, doi: 10.1002/aelm.202400698.

[54] W. Banerjee, X. Xu, H. Lv, Q. Liu, S. Long, and M. Liu, “Variability improvement of TiOx/Al2O3 bilayer nonvolatile resistive switching devices by interfacial band engineering with an ultrathin Al2O3 dielectric material,” *ACS Omega*, vol. 2, no. 10, pp. 6888–6895, Oct. 2017, doi: 10.1021/acsomega.7b01211.

[55] Y. Huang, Y. Luo, Z. Shen, G. Yuan, and H. Zeng, “Unipolar resistive switching of ZnO-single-wire memristors,” *Nanoscale Res Lett*, vol. 9, no. 1, pp. 1–5, 2014, doi: 10.1186/1556-276X-9-381.

[56] M. Ismail, C. Mahata, M. Kang, and S. Kim, “Exploring conductance modulation and implementation of convolutional neural network in Pt/ZnO/Al2O3/TaN memristors for brain-inspired computing,” *Ceram Int*, vol. 49, no. 11, pp. 19032–19042, Jun. 2023, doi: 10.1016/j.ceramint.2023.03.030.

[57] A. H. Jaafar and N. T. Kemp, “Light-Mediated Multilevel Neuromorphic Switching in a Hybrid Organic-Inorganic Memristor,” *ACS Omega*, vol. 9, no. 52, pp. 51641–51651, Dec. 2024, doi: 10.1021/acsomega.4c09401.

[58] M. K. Mahadevaiah *et al.*, “Modulating the Filamentary-Based Resistive Switching Properties of HfO2 Memristive Devices by Adding Al2 O3 Layers,” *Electronics (Switzerland)*, vol. 11, no. 10, May 2022, doi: 10.3390/electronics11101540.

[59] R. Khan, N. Ur Rehman, S. Iqbal, S. Abdullaev, and H. M. Aldosari, “Resistive Switching Properties in Memristors for Optoelectronic Synaptic Memristors: Deposition Techniques, Key Performance Parameters, and Applications,” Jan. 23, 2024, *American Chemical Society*. doi: 10.1021/acsaelm.3c01323.

[60] X. Chen *et al.*, “Flexible multilevel nonvolatile biocompatible memristor with high durability,” *J Nanobiotechnology*, vol. 21, no. 1, Dec. 2023, doi: 10.1186/s12951-023-02117-5.

[61] F. Gul and H. Efeoglu, “ZnO and ZnO1−x based thin film memristors: The effects of oxygen deficiency and thickness in resistive switching behavior,” *Ceram Int*, vol. 43, no. 14, pp. 10770–10775, Oct. 2017, doi: 10.1016/j.ceramint.2017.05.090.

[62] H. Lv *et al.*, “Atomic view of filament growth in electrochemical memristive elements,” *Sci Rep*, vol. 5, Aug. 2015, doi: 10.1038/srep13311.

[63] W. Chen *et al.*, “Essential Characteristics of Memristors for Neuromorphic Computing,” Feb. 01, 2023, *John Wiley and Sons Inc*. doi: 10.1002/aelm.202200833.

[64] L. Chua, “Resistance switching memories are memristors,” *Appl Phys A Mater Sci Process*, vol. 102, no. 4, pp. 765–783, Mar. 2011, doi: 10.1007/s00339-011-6264-9.

[65] Nathan R. McDonald, Robinson E. Pino, Peter J. Rozwood, and Bryant T. Wysocki, “Analysis of Dynamic Linear and Non-linear Memristor Device,” *IEEE Xplore*, Oct. 2010, doi: https://doi.org/10.1109/IJCNN.2010.5596664.

[66] J. Li, Z. Dong, L. Luo, S. Duan, and L. Wang, “A novel versatile window function for memristor model with application in spiking neural network,” *Neurocomputing*, vol. 405, pp. 239–246, Sep. 2020, doi: 10.1016/j.neucom.2020.04.111.

[67] Z. Biolek, D. Biolek, and V. Biolková, “SPICE Model of Memristor with Nonlinear Dopant Drift.”

[68] H. Abunahla and B. Mohammad, *Memristor Technology: Synthesis and Modeling for Sensing and Security Applications*. in Analog Circuits and Signal Processing. Cham: Springer International Publishing, 2018. doi: 10.1007/978-3-319-65699-1.

[69] J. J. Yang, D. B. Strukov, and D. R. Stewart, “Memristive devices for computing,” 2013, *Nature Publishing Group*. doi: 10.1038/nnano.2012.240.

[70] S. L. Johnson, A. Sundararajan, D. P. Hunley, and D. R. Strachan, “Memristive switching of single-component metallic nanowires,” *Nanotechnology*, vol. 21, no. 12, 2010, doi: 10.1088/0957-4484/21/12/125204.

[71] Peng Huang, Bin Gao, and Jinfeng Kang, “RRAM Device Characterizations and Modelling,” Jan. 2021. doi: https://libcon.rec.uabc.mx:2281/10.1007/978-981-15-6912-8_11.

[72] D. B. Strukov, F. Alibart, and R. Stanley Williams, “Thermophoresis/diffusion as a plausible mechanism for unipolar resistive switching in metal-oxide-metal memristors,” *Appl Phys A Mater Sci Process*, vol. 107, no. 3, pp. 509–518, Jun. 2012, doi: 10.1007/s00339-012-6902-x.

[73] M. A. Zidan, J. P. Strachan, and W. D. Lu, “The future of electronics based on memristive systems,” *Nat Electron*, vol. 1, no. 1, pp. 22–29, Jan. 2018, doi: 10.1038/s41928-017-0006-8.

[74] Z. Wang *et al.*, “Threshold Switching of Ag or Cu in Dielectrics: Materials, Mechanism, and Applications,” *Adv Funct Mater*, vol. 28, no. 6, Feb. 2018, doi: 10.1002/adfm.201704862.

[75] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, “Training and operation of an integrated neuromorphic network based on metal-oxide memristors,” *Nature*, vol. 521, no. 7550, pp. 61–64, May 2015, doi: 10.1038/nature14441.

[76] S. G. Kim, J. S. Han, H. Kim, S. Y. Kim, and H. W. Jang, “Recent Advances in Memristive Materials for Artificial Synapses,” Dec. 01, 2018, *Wiley-Blackwell*. doi: 10.1002/admt.201800457.