Universidad Autónoma de Baja California

Facultad de Ciencias

TOWARDS COVALENT ORGANIC FRAMEWORK FIELD EFFECT TRANSISTOR

Que para obtener el grado de

Maestra en Ciencias

Presenta

María Fernanda Herrera Martínez

Ensenada, Baja California, México, Abril 2025

UNIVERSIDAD AUTÓNOMA DE
BAJA CALIFORNIA
Facultad de Ciencias

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353711

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Acknowledgements

First of all, I would like to express my sincere gratitude to the Universidad Autónoma de Baja California, which, since the beginning of my time at this institution, seven years ago, has marked a great improvement in my journey as a physicist. In addition, this journey would not have been possible without the economic support of CONAHCYT, which financed my research.

I would like to thank my thesis supervisors, Prof. Jan Mol and Dr. Ramon Carrillo Bastos, for all their support, knowledge, patience, and guidance throughout this project. To Dra. Eloisa del Carmen Garcia Canseco for her support during my first semester of my master's degree and her endless encouragement.

To my Comitee Dra. Priscilla Elizabeth Iglesias Vazquez and Dr. Jorge Alberto Villavicencio Aguilar for their valuable input and for guiding the project into the right direction.

This thesis is a reflection of the endless support and love I have received from my family during this challenging academic pursuit. I am forever grateful to my parents, who have always pushed me to follow my dreams and nurtured my curiosity and passions.

To my whole heart, Israel, your endless patience and understanding, especially during the most demanding and challenging phases of this master's degree, have been my anchor.

Abstract

The urge to make things smaller and more efficient in the world of advanced electronics has driven tremendous innovation in nanotechnology. A key technological advancement seen in nanotechnology is the use of field-effect transistors, which allow good control over electronic signals at a nanoscale level, underpinning the digital revolution. Although silicon is still the semiconductor of choice for these devices, there has been a growing interest in alternative materials as we approach the limits of Moore's law. In this project, our aim is to create a field-effect transistor device composed of a two-dimensional Covalent triazine framework-1 material. These frameworks, if appropriately chemically engineered, can exhibit interesting electronic structure characteristics such as Dirac cones and flat bands.

A big challenge in making use of these properties is the integration of these materials into the device itself. In addition, though covalent triazine framework-1 has a tunable band gap and a porous structure ideal for semiconductors, variations in thickness indicate poor consistency in fabrication in one sample to another.

Our experiments using atomic force microscopy have demonstrated that using higher concentrations of materials during the making of devices leads to better electrical conductivity. This finding confirms that how much material we use is key to increasing the performance of devices based on the covalent triazine framework-1.

Using the correct concentration, we were able to coat another chip, one fitted with a pattern of interdigitated spaced electrodes. That was an important first step in that it is planned to extend this methodology to smaller surface area devices, but it was considered important to verify that we could start by fabricating a larger surface area device.

We observed that the metal oxide-semiconductor field-effect transistors not only behaved as expected when we tested their current against voltage, but they also conducted electricity better at higher gate voltages. However, the presence of some electrical noise and inconsistent

currents suggests that we still have some corrections to do with the covalent triazine framework-1 material to get optimal performance.

The next step was to reduce the surface area configuration in the electrode surface, and while initial results showed typical metal oxide-semiconductor field effect behaviour with gate voltage modulating current, the averaged data revealed unexpected behaviour where conductivity remained unchanged across gate voltages, likely due to charge trapping within the covalent triazine framework-1 material. Finally, for the last sample, the surface area was even further reduced, with electrodes patterned onto a single Covalent triazine framework-1 flake. In this sample, we encountered difficulties in accurately locating the flakes during thermal scanning lithography; however, despite these challenges, successful patterning in the Covalent triazine framework-1-Poly(methyl methacrylate)-Polyphosphoric Acid stack was achieved, suggesting that the process remains viable for future device development with improvements in material synthesis and deposition.

Keywords: Field-effect Transistor, Electrical conductivity, device fabrication, semiconductors, covalent triazine framework-1, gate, current, voltage.

Chapter 1

Motivation

The push to make electronic devices smaller and more efficient has been at the heart of modern nanotechnology's progress. A key outcome of this has been the development of nanodevices, especially field effect transistors (FETs). These transistors are fundamental to modern electronics, providing accurate control over electrical signals at extremely small scales, a key element in the digital revolution [1]. As technology progresses, reducing the size of these devices allows the integration of more transistors onto a single chip, thereby improving performance and energy efficiency [2]. For example, current microprocessor chips can contain up to 10 billion transistors, each featuring a gate length of only a few nanometres [3].

Nanotransistors play a critical role in handling electrical signals on such a tiny scale, but even with all the advancements in 2D transistors, we're still exploring their full potential. While it's clear that these transistors are becoming more powerful and versatile, their complete range of applications and limitations hasn't been fully mapped out yet. That's why reviewing the core principles and performance of 2D transistors is important—to better understand what they're capable of and where they might be used in the future.

Silicon has traditionally been the dominant material in semiconductor devices because of its excellent electrical properties and mature manufacturing processes. However, as the physical and economic limits of silicon technology, as foreshadowed by Moore's law, are approached, the usage of alternative materials is being increasingly explored. Moore's law refers to a prediction that the number of transistors on integrated circuits will approximately double every 18 months and has conventionally driven the advancement in the semiconductor industry for many decades. This was traditionally achieved by rapidly scaling down the size

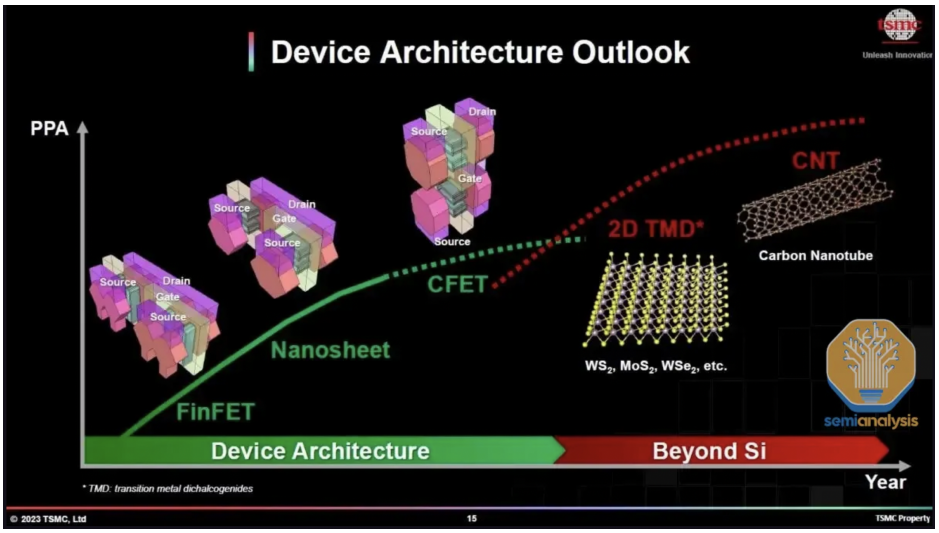


Figure 1.1: Device Architecture Outlook showing the progression from FinFET to CFET and beyond, including 2D materials and carbon nanotubes [**INTEL**].

of transistors from micrometres to a few nanometres today, so as to increase the density of the transistor in integrated chips [4, 5].

As transistor dimensions approach the atomic scale, quantum mechanical effects and other challenges threaten the continuation of Moore's law. Fig. 1.1, shows a roadmap of semiconductor technologies, from current FinFET devices to future architectures such as nanosheets, CFETs, and beyond-silicon materials (2D TMDs and carbon nanotubes [6, 7, 8]). It highlights how such improvements and advances could maintain the pace of Moore's law through improving the efficiency in power performance and through the integration density. This has re-ignited interest in studies on 2D materials such as graphene, molybdenum disulphide (MoS_2), and covalent organic frameworks that promise prospects of unique electronic properties which will be capable of stretching limits that no other traditional semiconductor technology is capable of [9]. These new materials, combined with the development of 2D transistors, may allow the continuation of a Moore's law trajectory and may provide new opportunities in device design and functionality.

Chapter 2

Background

2.1 Transistors

Transistors sparked a revolution in electronics nearly 80 years ago and have been previously called "one of the most important inventions of the 20th century". Today, we can expect transistors to be present in our smartphones, tablets, computers, and other electronics that are crucial to the world we live in today [10].

Transistors are devices made from semiconducting materials that work by regulating the height of an energy barrier with an applied voltage, preventing electrons from flowing from the source to the drain. Transistors can also amplify and generate electronic signals that act as switches. However, in this specific research we focus on a metal oxide-semiconductor field effect transistor (MOSFET), with a 2D material between the contacts and the semiconductor material 2.1.

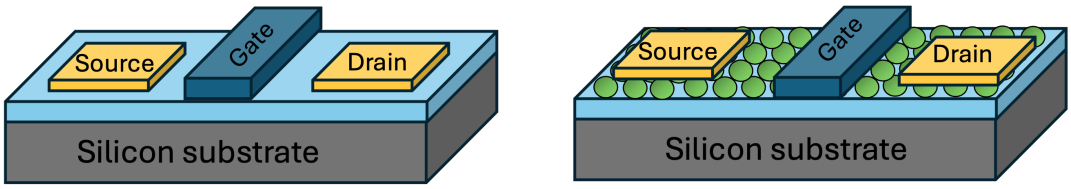


Figure 2.1: Illustration of a typical metal oxide-semiconductor field effect transistor and a metal oxide-semiconductor field effect transistor with a 2D material between the contacts and the substrate.

2.1.1 Metal-oxide-semiconductor field-effect transistor (MOSFET)

The simplified basic configuration of a MOSFET is given in Fig. 2.2. Typically, MOSFETs are p-type semiconductors, into which two n+ regions (source and drain) are implanted by ion implantation. The gate electrode commonly consists of doped polysilicon or silicide and serves to control the channel between the source and the drain. SiO_2 is the usual gate oxide and acts as a physical insulator between the channel and the gate. If a voltage is applied to the gate, an inversion layer is formed in a semiconductor so that a conductive link between the source and the drain is allowed. Modulation of channel conductivity can be done by changing the gate voltage or by variations in contact between the surface and the back (substrate) [11].

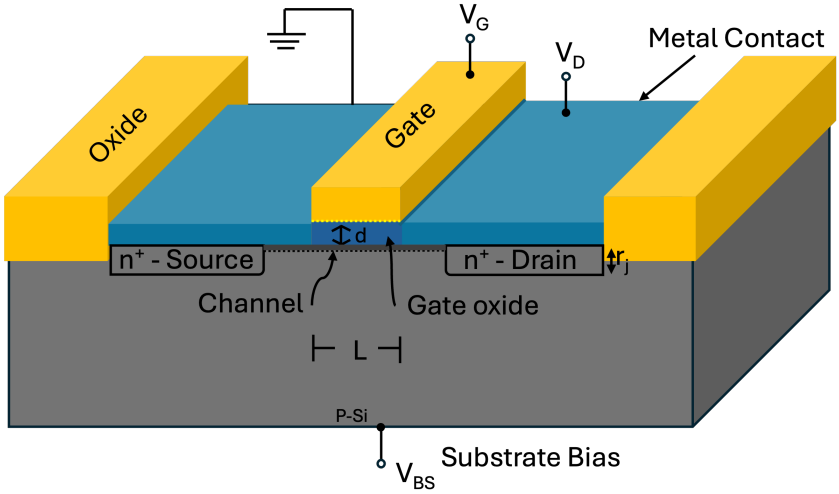


Figure 2.2: Illustration of a metal-oxide-semiconductor field-effect transistor.

At this point, the MOSFET is in the ohmic or linear region. In this region it follows Ohm's law, as the voltage increases, the current increases linearly. However, as the voltage increases, the depletion region between the drain and the substrate increases as they are reverse-biased. The channel also begins to deplete towards the drain end because the drain is at a positive potential and negative charges from the channel closest to the drain are pulled into the drain. This reduces the width of the channel, restricting the flow of charges and reducing the flow current to reach a saturated region (Fig. 2.3).

In the case of an applied voltage between the source and drain terminals, the MOS structure is out of equilibrium, and the minority carriers will form an n-type conductive channel. The quasi-Fermi level of the gate voltage is reduced, which symbolises the electron populations in the conduction and valence bands. Equilibrium means that, without any gate

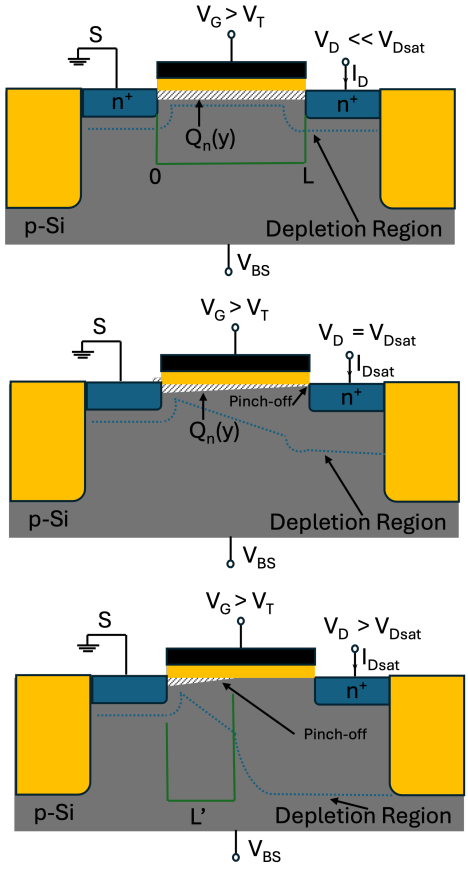


Figure 2.3: MOSFET operatad in the linear region, at onset saturation and beyond saturation (effective channel is reduced).

bias, no channel is formed. When a sufficiently positive voltage is applied to the gate, a surface inversion layer develops [11].

Figure 2.3 also illustrates key physical aspects of this process. The term $Q_n(y)$ denotes the inversion charge sensity along the lenght of the channel, from the source (at $y = 0$) to the drain (at $y = L$). The green lines represent the effective channel lenght, which shortens from L to L' in deep saturation as the pinch-off point shifts towards the source. The blue dotted lines outline the depletion regions that expand with increasing voltage. Together, these elements help visualize the progressive narrowing of the channel and eventual formation of a pinch-off region as the MOSFET transitions into saturation [11].

The inversion layer forms when the surface potential (ψ_s) satisfies the following condition:

$$E_{Fn} - E_i = q\psi_s$$

where E_{Fn} is the Fermi level, E_i is the intrinsic Fermi level, and ψ_s is the surface potential.

In inversion, the surface potential is

$$\psi_s = 2\psi_B$$

where ψ_B is the potential required for weak inversion. For strong inversion, the gate voltage must be even higher, ensuring a sufficient charge for conduction.

The inversion charge per unit area at the onset of inversion Q_i can be approximated by:

$$Q_i \approx C_{ox}(V_{GB} - V_T - 2\psi_B)$$

where C_{ox} is the oxide capacitance, V_{GB} is the gate-to-bulk voltage, and V_T is the threshold voltage. This equation shows that increasing the gate voltage above the threshold also increases the inversion charge, strengthening the conductive channel between the source and the drain.

This pinch-off point occurs because the voltage difference between the gate and the semiconductor decreases. At this stage, the drain voltage and current are named $V_{D,sat}$ and $I_{D,sat}$, respectively (see Fig. 2.4). After the pinch-off point, the current remains constant regardless of V, indicating the saturation region [11].

2.1.2 Current Voltage for a FET

I–V measurements are a key electrical characterisation method in the analysis of FET operation. They also give insights into qualitative and quantitative intrinsic semiconductor characteristics relating to mobility and carrier density, but also external characteristics such as interface states and contact resistance. Up to this date, the measurement methodologies for 2-point probe technique (2PP) involve current and voltage applied and measured by the same set of terminals. This methodology has become the standard method of determining the output and transfer characteristics of the 2D FET [12, 11].

Output Characteristics

The output characteristics are determined by sweeping the drain-to-source gate (V_{DS})voltage across a specified range in defined increments while keeping the gate-to-source voltage (V_{GS}) constant. This process highlights the FET's operational regions, including the linear, saturation, and subthreshold regions, as well as the device's ability to handle current flow at

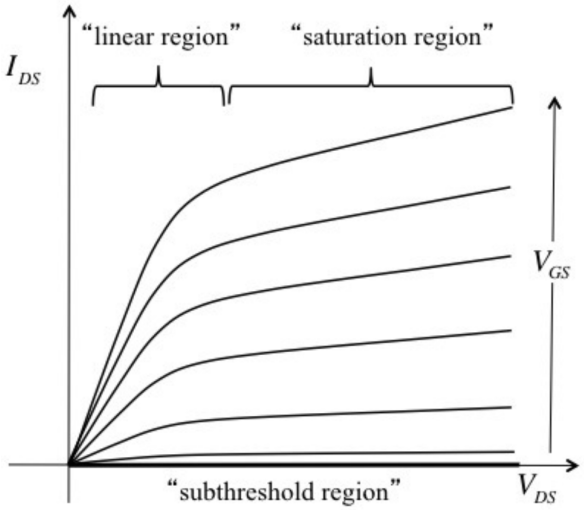


Figure 2.4: Idealized drain characteristics for a MOSFET (I_D vs V_D). The dashed lines separate the regions: linear, nonlinear and saturation.

different drain voltages. A voltage is applied to the device gate and the drain voltage is swept through the required range, also in increments, while measuring the drain current at each corresponding drain voltage point. For FET output measurements, the drain current is recorded as a function of V_{DS} at different gate voltages V_{GS}. The plots can then be made from these data to show V_{DS} - I_{DS} with curves corresponding to each of the specified gate voltage levels [12, 13].

Transfer Characteristics

Another way of assessing the electrical performance of an FET is by transfer characteristics obtained by measuring the drain current (I_D), as a function of the gate-to-source voltage (V_{GS}), keeping the drain-to-source voltage, (V_{DS}), constant. This relationship demonstrates how variations in the gate voltage directly influence the current flow through the device, emphasizing the control capability of the gate over the channel. The transfer characteristic of MOSFET devices reflects the relationship between the drain current (output) and the gate voltage (input). The standard transfer test for n-type MOSFET includes the application of a constant voltage to the drain and the removal of the gate bias from a little negative to a positive bias [12, 13].

2.1.3 MOSFET Structures

MOSFETs have been fundamental to the electronics industry, but as channel lengths shrink to less than 10nm, performance issues arise that require novel design approaches. Constant field scaling is the simplest way to manipulate short-channel effects in MOSFET. Since a large factor in short-channel effects is the effect of an increase in field strength at low voltage, the same argument could be applied when discussing shrinking all dimensions and voltages equally by a factor (κ) thereby keeping steady-state internal E fields. However, this approach has its limitations, since some physical properties (e.g. junction voltage and surface potential) do not scale down so smoothly. In addition, for devices that are shrunk down to really small dimensions (in the nanometre regime), other issues like quantum effects and oxide no-longer-thick layers contribute some of their own problems. Some strategies include advanced doping profiles, gate stacks, and source / drain structures to address short channel effects [11].

- **Channel Doping Profile:** For most high-performance MOSFETs, the channel region has a retrograde doping profile: the peak doping concentration is just below the semiconductor surface. This helps with short-channel effects by reducing punch-through and the threshold voltage. Low doping at the surface allows better carrier mobility, while heavy doping deeper in the channel reduces undesirable current leakage. The profile tends to reduce junction capacitance and manage threshold voltage more effectively. [14, 15, 16, 11].

- **Gate Stack:** The gate stack includes the gate dielectric and the gate contact. Conventional SiO_2 has given way for High-$\varkappa$ dielectrics, allowing the use of thicker oxides with less tunneling, which can raise the efficiencies of devices. Materials like HfO_2, and even TiO_2 layer, have provided ways for a dielectric layer to be thicker without sacrificing capacitance. However, poly-Si still represents the default gate material owing to compatibility with silicon processing but has a few disadvantages like higher resistance and thinning at the oxide interface. Further optimization of the device against n-type or p-type applications can be attained by work function tuning of the gate. However, especially while shrinking the gate dimensions, the resistance of poly-Si is becoming a challenge [17, 18, 11].

- **Source/Drain Design:** The innovations in source/drain design are imperative with

respect to the control of series resistance and minimizing short-channel effects. Silicide contacts decrease the resistance between the metal contact and the silicon channel. Self-aligned silicide process decreases sheet resistance, hence minimizing losses between gate and channel. Another approach is that of Schottky-barrier source/drain, but they possess higher series resistances and problems linked to drain leakage. In raised source/drain designs, the epitaxial layer grown over source and drain regions assists in constraining the junction depth for reduction in short-channel effects [19, 20, 11].

Each of these methods addresses short-channel effects, which supports performance while scaling down the MOSFET devices further. These include sophisticated structures like high-$\varkappa$ dielectrics, retrograde doping profiles, and silicide contacts that will allow further improvements in active operation with reduced channel lengths. There are other methods that target this, such as silicon on insulator (SOI) and thin film transistor (TFT), three-dimensional structures, and power MOSFETS [11].

2.2 Integrating 2D Materials into Device Fabrication Processes

Since their invention in 1959, MOSFETs have continually been scaled down, putting a demand on careful design to retain long-channel characteristics [3, 21]. For shorter channels, punch-through between source and drain might occur, which requires greater channel doping. However, with higher doping, the threshold voltage increases, and hence the need to reduce the oxide thickness. Various device parameters are interrelated; Optimal performance is maintained by scaling rules. Similarly, despite those prescriptions, the short-channel effects are unavoidable. These arise owing to complex two-dimensional electric fields in the channel and thus form a deviation from the ideal long-channel behaviour. Stronger electric fields lead to mobility degradation, velocity saturation, and related parasitic effects such as hot carrier injection. In summary, short-channel effects alter the basic parameters of threshold voltage, current saturation, and general lifetime of the device; hence, they complicate the scaling of MOSFETs [22, 23].

Rather than scaling silicon electronics, continuous improvement is expected to come from the incorporation of new materials that can push the boundaries of silicon electronics longer [24]. However, most electronic materials are non-2D materials, scalability of which is an issue.

For example, when such materials are reduced to atomic layer thickness, we expect undesirable variations in electrical properties. All atoms that make up these part-materials differ in their characteristics from other non-2D materials by the novelty of atomic layer structures that possess [25, 26, 27]. Unlike non-2D materials, 2D materials have atomic layer structures that possess prime electrical, optical, and mechanical properties such as high carrier mobility, excellent electrical conductivity, and tunable band structures [28].

Hence, to determine the optimum semiconductor materials for transistors, one should conduct an analysis of electrostatics in an FET, as determined by Poisson's equation.

$$\frac{d^2\phi(x,y,z)}{dx^2} + \frac{d^2\phi(x,y,z)}{dy^2} + \frac{d^2\phi(x,y,z)}{dz^2} = \frac{qN_a}{\epsilon_b}$$

where $\phi(x,y,z)$ is the potential distribution in the channel, N_a is the doping concentration and ϵ_b is the doping concentration. By solving Poisson's equation with boundary conditions assuming $z = 0$ (surface potential) and that y is sufficiently large (for wide devices), we can simplify the above equation into a one-dimensional form.

$$\frac{d^2\Phi(x)}{dx^2} - \frac{\Phi^2(x)}{\lambda^2} = 0 \quad \text{with} \quad \lambda = \sqrt{t_b t_{ox} \epsilon_b / \epsilon_{ox}}$$

Generally speaking, it is viewed that the gate length for a standard metal-oxide-semiconductor field-effect transistor should be 5-10 times larger than the characteristic length to provide enough gate control and low OFF-state leakage current. This has also been further confirmed by quantitative analysis and numerical simulations [5].

By analyzing the above equation, we can deduce that as the channel length of a transistor is reduced, the thickness of the semiconductor body (tb) should also be reduced [29]. However, ultra-thin-body (UTB) semiconductors created by thinning three-dimensional (3D) bulk materials often face significant challenges due to non-ideal structural termination, including rough surfaces and unavoidable surface/interface dangling bonds.

2D materials form a very important part of SOI and TFT. In SOI technology, the top silicon layer is a high-quality single-crystalline material and therefore an ideal choice for realising high-performance and high-density circuits. Several types of SOI structure have been developed: SOS (silicon-on-sapphire), SOZ (silicon-on-zirconia), and silicon-onoxide (also called silicon-on-nothing or air gap). The most common SOI material is silicon on silicon

dioxide (Si on SiO_2 on Si), where a thin silicon layer is separated from the silicon substrate by a buried oxide (BOX) layer [11, 30]. The insulating layers in such designs are materials like Al_2O_3 (SOS) or ZrO_2 (SOZ) [30], in which a silicon film is grown on a crystalline substrate. The problem facing these technologies is maintaining material quality as the thickness is reduced. The key advantages of SOI MOSFETs and TFT are that the substrate provides isolation for the thin body, provides better punch-through control, lower parasitic capacitance, and allows higher operating speeds. This will enhance the circuit density without latching. Higher costs and limitations in thermal conductivity are possible drawbacks of this device [31, 11].

2.2.1 Graphene devices

In addition to traditional 3D bulk semiconductors, there is a wide range of two-dimensional semiconductors consisting of covalently bonded lattices that are only one or a few atoms thick. These two-dimensional semiconductors have surfaces free of dangling bonds, which allows them to retain excellent electronic and optical properties even at single-atomic thicknesses [32], in stark contrast to conventional bulk semiconductors, which suffer from dangling bonds and trapped states at surfaces and interfaces [29, 33]. Since 2004, significant research has focused on graphene, the "original" 2D material, which has revealed intriguing electronic and photonic properties [34, 35, 33, 36, 12]. Two-dimensional Van der Waals materials, such as graphene, have shown great potential for next-generation electronics. However, graphene's lack of an energy bandgap (Fig. 2.5) limits its use in radio frequency electronics and makes it unsuitable for digital electronics, which require both high on-state currents and low off-state currents [37].

The output characteristics of many graphene MOSFETs (Fig. 2.6) show a linear shape without any saturation or only weak saturation, each of which is a disadvantage with respect to the speed of the device [39].

For example, the work seen in [41]. In these graphene field-effect transistors (GFETs), electron transport dominates at positive gate voltages and hole transport at negative gate voltages, with the conductance minimum, known as the Dirac point, occurring where electrons and holes contribute equally to transport. Fig. 2.7 shows the output characteristics n-type (I_D-V_D) of the graphene transistor at different gate voltages. The absence of current saturation

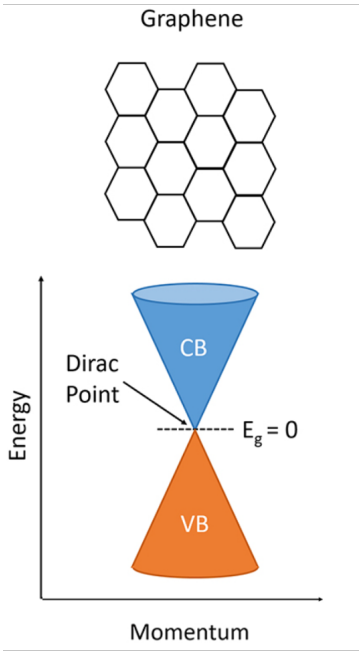


Figure 2.5: Schematic band structures of Graphene. Retrieved from [38]

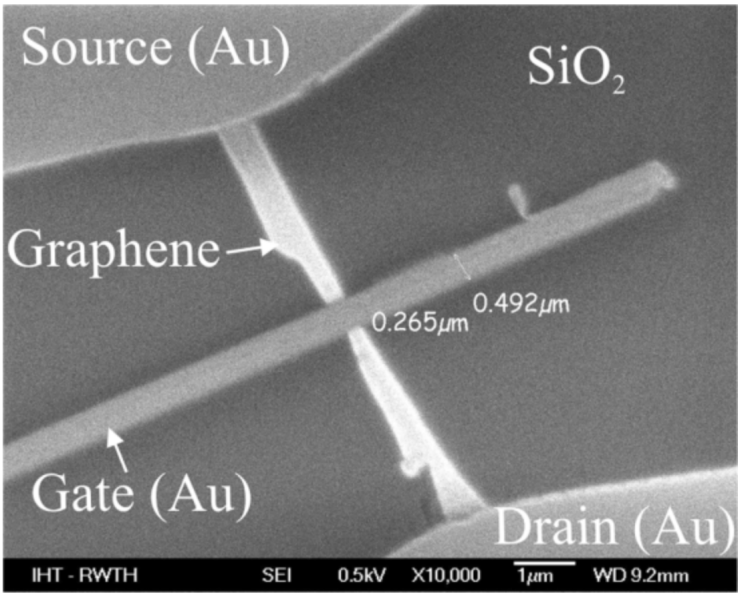


Figure 2.6: Scanning electron microscope (SEM) image of the FET. The graphene flake's length from source to drain is L=7.3 μm, width of W=265 nm at the gate region, and a gate length of L=500 nm. The graphene's thickness was mesured by atomic force microscopy and it is t=1.5 nm. Retrieved from [40]

seen is attributed to the fact that graphene is a zero-gap semiconductor. Although velocity saturation at higher biases has been proposed to result in current saturation in graphene transistors, achieving this may require higher carrier mobility within the practical drain bias range.

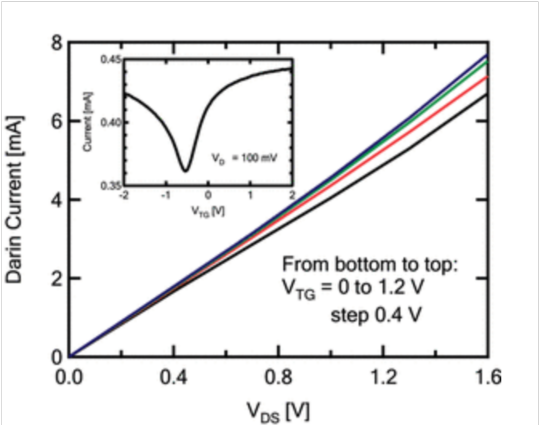


Figure 2.7: Measured output characteristics of the graphene transistor for various top-gate voltages. The inset shows the transfer characteristics at a drain voltage of 100 mV. Retrieved from [39]

As a result, researchers have turned their attention to other two-dimensional semiconductors [29, 42, 36, 43, 40].

2.3 Covalent Organic Frameworks

Covalent organic frameworks (COFs) are a class of crystalline materials composed of light elements such as hydrogen, boron, carbon, nitrogen, and oxygen, which are covalently bonded together to form highly ordered porous networks, a major advantage for promising applications [44], specifically in electronic devices (see Fig. 2.8).

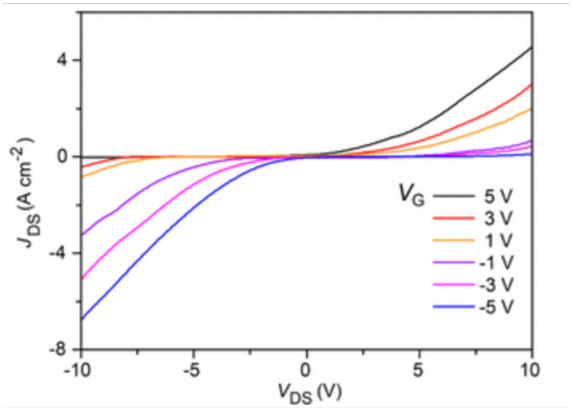


Figure 2.8: Output characteristics of the ambipolar SLG/COFTFPy-PPDA-VFET depending on various gate voltages. Retrieved from [45]

Band theory has helped us to understand the fundamental properties of inorganic crystalline materials, which can also be used to better understand COFs.

2.3.1 Implementation of CTF-1 into FETS

Covalent triazine frameworks-1 (CTF-1) are a class of porous organic polymers and represent one of the most interesting classes of covalent organic frameworks. These materials are highly ordered and contain porosity, with well-defined micro- and mesopores typically ranging between 0.5–2 nm [46, 14]. The pore size and dispersity of CTF-1 can vary depending on the fabrication method, with ionothermal synthesis often yielding uniform pores, while other methods, such as solvent-assisted or mechanochemical approaches, may result in a broader pore size distribution [47, 48, 14]. Ionothermal methods using molten salts like zinc chloride are particularly effective for producing highly porous frameworks with surface areas exceeding 2000 m^2/g and consistent pore structures [46]. This high porosity and structural order make CTF-1 particularly suitable for applications in gas storage, separation, and catalysis [49, 2]. CTF-1 is constructed using triazine rings as the main building blocks. Triazine is a heterocyclic organic compound rich in nitrogen, which allows it to have high thermal and chemical stability. Covalent bonds between triazine units provide a rigid and stable framework [50].

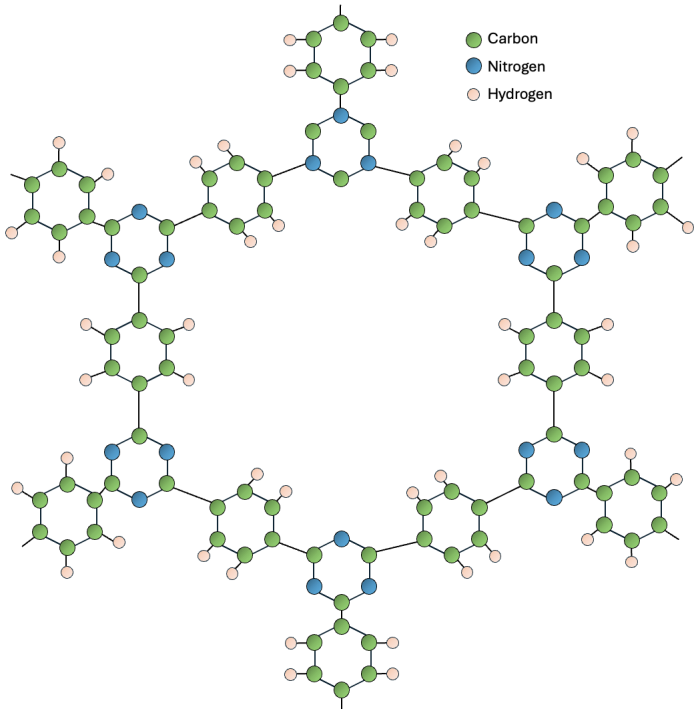


Figure 2.9: Structure of a Covalent Triazine-Based Framework CTF-1.

Band structure

A conjugated π-system consists of delocalised electrons in several atoms, allowing electron mobility throughout the structure [51, 52]. This type of polymer is of particular interest due to its band structure [53]; its band structure can be manipulated by changing its building blocks without changing the main properties of these polymers, such as Dirac cones.

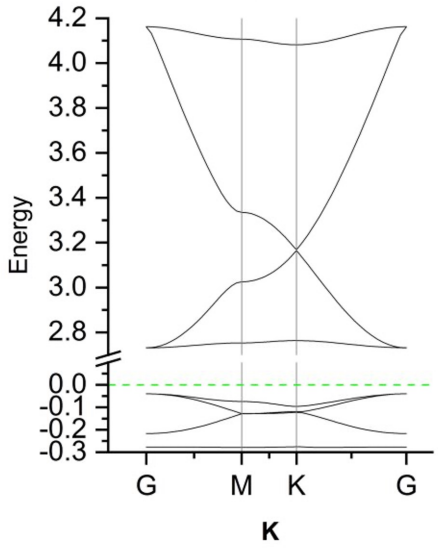


Figure 2.10: Band Structure of CTF-1. Image and analysis of the band structure by Rebecca Peake, phD of my research group.

As shown in Fig. 2.10, it seems that the band gap allows the electron to make a direct transition between these bands without any change in momentum. The bands near the K point have a linear dispersion relation and meet at a single point. In fact, this speaks for the possibility of hosting Dirac cones, similar to those in graphene, which signal high electron mobility.

CTF-1 has a strong absorption peak in the UV region, especially in the range around 300-400 nm, as shown in Fig. 2.11, which gives evidence of the strong absorption of UV light from CTF-1 characteristically for materials with a band gap in the near-UV to visible range. In FETs, a large bandgap material usually has a low intrinsic carrier concentration at room temperature, which can potentially reduce the leakage current, thus giving rise to the on/off ratio of a transistor. Beyond UV, the absorption drops, with absorption being very low in the visible region from 400-700 nm. This implies that CTF-1 is very poor at visible light absorption, which could be caused by a relatively large band gap and could make this

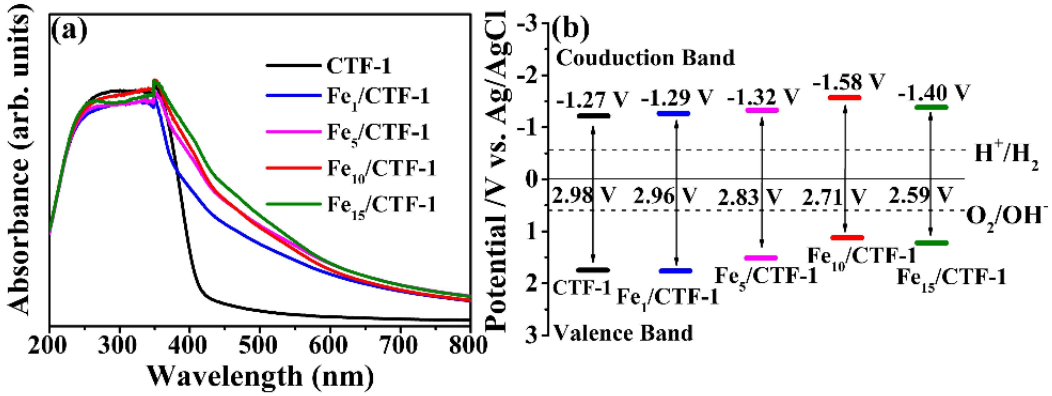


Figure 2.11: a) UV/Vis DRS of CTF-1 and Fex/CTF-1 samples and b) schematic illustration of band structures of CTF-1 and Fex/CTF-1 samples. Retrieved from [53]

compound suitable for operating systems in applications requiring UV light absorption.

CTF-1 has a valence band edge at approximately 2.98 eV vs. Ag/AgCl. This is the potential at which the electrons are in the ground state before being excited to the conduction band; this indicates that holes (positive charge carriers) in CTF-1 are energetically stable, which may influence the threshold voltage required to induce hole conduction in a p-type FET. The energy difference between the valence band and the conduction band gives the band gap of the material. For CTF-1, the band gap can be deduced from these values, although it is not directly given in energy units (eV). The large difference between the edges of the conduction and valence bands suggests a significant band gap, which is consistent with UV-Vis absorption data, where CTF-1 absorbs predominantly in UV.

The absorption maximum for CTF-1 appears near $300 - 350nm$ (Fig. 2.11), which corresponds to an energy range of approximaetly $3.5 - 4.1eV$, based on the relationship $E = \frac{hc}{\lambda}$. This is higher than the estimated optical bandgap from the UV/Vis onset and from the band structure analysis. The reason for this discrepancy is that the absorption maximum corresponds to the most probable electronic transition, which is not necessarily the lowest energy (i.e., bandgap) transition. Additionally, factors such as excitonic effects, transitions involving higher-energy electronic states, or localized $\pi - \pi$ transitions within the conjugated framework may contribute to this higher energy absorption peak. Therefore, the absorption maximum being greater than the bandgap is a common phenomenon in conjugated organic frameworks like CTF-1.

Chapter 3

Objectives and Hypothesis

In this project, we wanted to design an FET device using a sample of two-dimensional COFs. One of the major challenges involves integrating these materials into devices and seeing if they actually behave as a MOSFET.

We propose that a device can be created on a silicon dioxide substrate by drop-casting monolayers of CTF-1 on the substrate and then patterning electrodes onto the sample. Furthermore, we claim that CTF-1 can be deposited on chips featuring interdigitated electrodes to create a functioning device. We anticipate that the resulting device will show standard output and transfer characteristics akin to those observed in a successful MOSFET. Specifically, we anticipate:

For the output characteristics:

1. The linear region, at low values of V_{DS}, I_D increases with an increase in V_{DS} provided that V_{GS} remains constant.

2. The saturation region for higher values of V_{DS}, where I_D becomes constant or stable and thus is primarily dependent on V_{GS}. This behavior is expected because, at higher V_{DS}, the charge carriers in CTF-1 reach their maximum transport capacity, and further increases in V_{DS} no longer lead to significant increases in current. The saturation occurs due to the limited mobility of charge carriers and the intrinsic properties of CTF-1, where the current is controlled mainly by VGS, and the material's conductivity is saturated.

For the transfer characteristics:

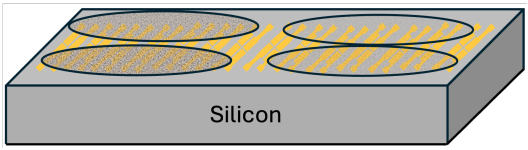
1. A threshold voltage (V_{th}) at which the device initiates conduction.

2. After the threshold voltage, the drain current, I_D, increases exponentially as we increase the gate voltage V_{GS} showing good gate control.

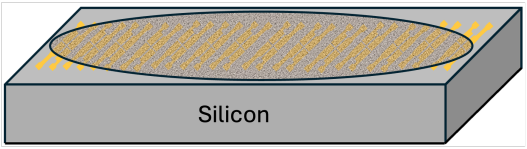
Chapter 4

Methodology

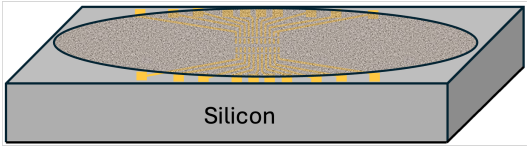
The analysis is divided into four different samples.



(a) Sample 1. Device fabricated by depositing different concentrations of CTF-1 solution on silicon dioxide (SiO_2)



(b) Sample 2. Device fabrication by CTF-1 solution deposition on silicon dioxide (SiO_2) chip with interdigitated electrodes



(c) Sample 3. Device fabrication by CTF-1 solution deposition on silicon dioxide (SiO_2) with electrodes concentrated in a smaller area

(d) Sample 4. Device fabrication on silicon dioxide (SiO_2) with contact onto an individual flake of CTF-1 solution

Figure 4.1: Illustration of the device fabrication methodologies used for CTF-1 deposition on silicon dioxide (SiO_2) with different electrode configurations.

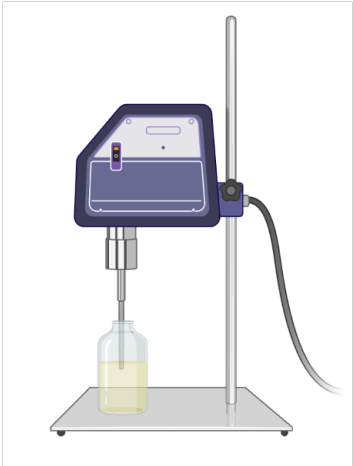
4.1 Solution preparation

The CTF-1 solution was prepared according to [54], where CTF-1 powder is mixed with deionized water as the solvent. Synthesis was kindly provided by my research team colleague Rebecca Peake. To this end, it should be noticed that the sample was synthesised around 16 months ago, and since then it has been kept in a cool and dry place.

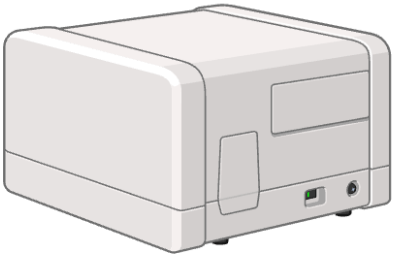
4.2 Material Characterisation

For the analysis of this solution, a high-power probe sonicator was used, we sonicated the solution for 5 minutes. We wanted to analyse how the UV-Vis spectra changed as the sonicated sample ages. We wanted to characterise the absorbance or transmittance through the liquid over a range of wavelengths.

Ultraviolet-visible (UV-Vis) spectrophotometers work by using a light source to shine light on a sample, covering wavelengths from the UV to the visible spectrum (typically 190 to 900 nm). The device measures how much light is absorbed, transmitted, or reflected at each wavelength by the sample. Some spectrophotometers also extend into the near-infrared (NIR) region, ranging from 800 to 3200 nm [55, 56]. The results we expect to see are shown in Fig. 2.11.



(a) Illustration of Probe Sonicator and sample of CTF-1



(b) Illustration of equipment used to do the absorption analysis wwith UV-Vis spectra

Figure 4.2: Illustration of process followed to analyse the CTF-1 Solution.

4.3 Sample 1. Device fabricated by depositing different concentrations of CTF-1 solution in silicon dioxide (SiO_2) with interdigitated electrodes

The sample was prepared by depositing 4 different concentrations of CTF-1 solution in a silicon chip that had interdigitated electrodes. The concentrations used were as follows:

C_1 = 0.1 mg/mL of CTF-1.

C_2 = 0.0025 mg/mL of CTF-1.

C_3 = 0.00025 mg/mL of CTF-1.

C_4 = 0.000125 mg/mL of CTF-1.

After deposition, the sample was air dried for about 24 hours. The main reason for this was to determine the concentration that would serve best for device fabrication regarding the uniformity which the deposited layers would be in, and how they would interact with the electrodes.

4.4 Sample 2. Device fabrication by CTF-1 solution deposition on silicon dioxide (SiO_2) chip with interdigitated electrodes

Upon determining the ideal concentration from Sample 1, we proceeded to create a second device by applying this concentration by dropcasting it onto another chip with interdigitated electrodes. The sample chip was prepared by dropping the solution C_1 from the previous sample directly onto the surface. This arrangement contained meander line electrodes. Lastly, the sample was air-drying for approximately 24 hours. The large surface area of the interdigitated configuration continued to offer high reliability for contact with CTF-1 flakes as it ensures that at least one of the electrodes will contain flakes of this material.

4.5 Sample 3. Device fabrication by CTF-1 solution deposition in silicon dioxide (SiO_2) with electrodes concentrated in a smaller area

With the optimal concentration established, our goal was to minimise the surface area covered by the electrodes.

In this iteration, the same concentration of CTF-1 (concentration C_1) was deposited on a chip where all electrodes were concentrated in the central region. This configuration was chosen to investigate the material response in a more localised region of the chip. The interdigitated electrodes used in the earlier samples covered a large area, making it highly likely that the material was being measured. However, this smaller, concentrated electrode

design aimed to explore whether similar electrical behaviour could be achieved with a more focused measurement area. The thickness of the silicon chip was 500 nm and had a layer of 275 nm thick SiO_2.

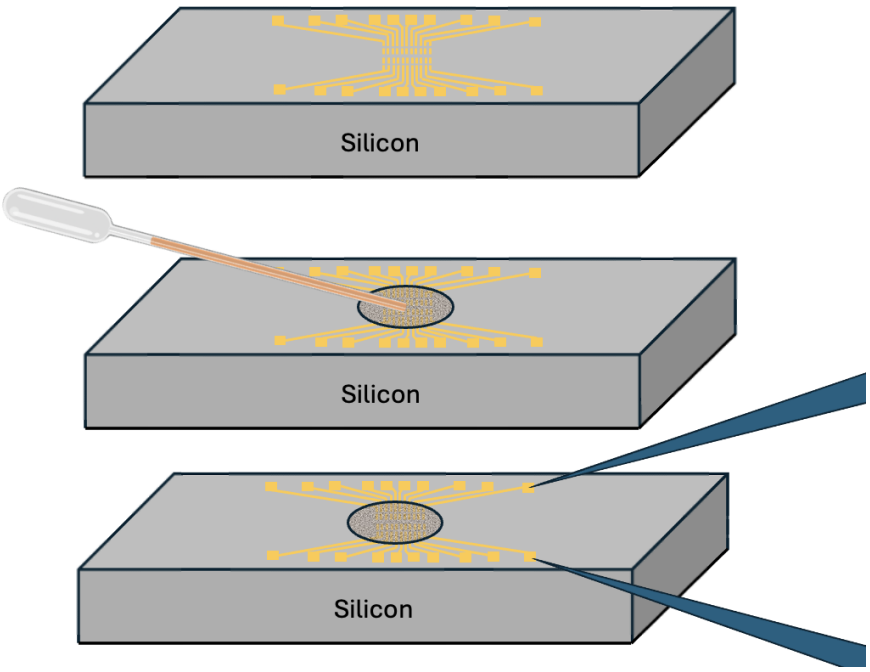


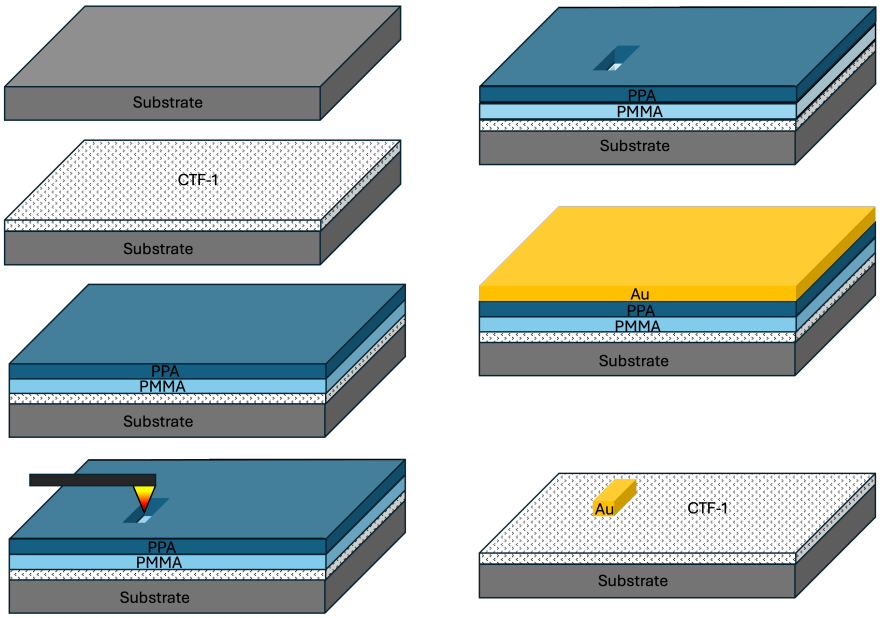
Figure 4.3: Illustration of device fabrication by CTF-1 solution deposition in silicon dioxide (SiO_2) with electrodes concentrated in a smaller area.

4.6 Sample 4. Device fabrication on silicon dioxide (SiO_2) with contact onto an individual flake of CTF-1 solution

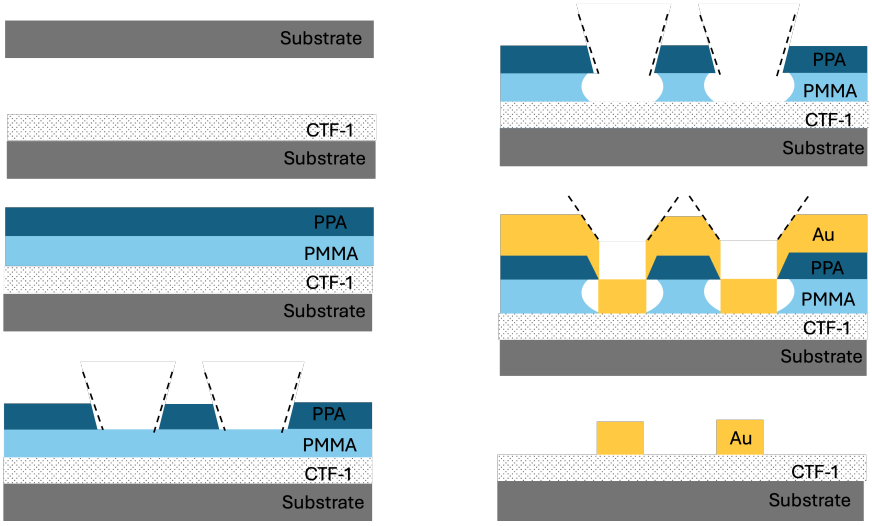
In the final sample, we further improved the fabrication by first drop-casting the CTF-1 solution onto the chip and then patterning the electrodes directly onto an individual flake of the material. This route was taken with regard to characterising its electrical properties in a specific well-defined area of the material.

The device was prepared by a process called the bilayer lift-off (BLO) process. This process is especially favourable if one wants to make high-quality electrical contacts. It consists of 4 steps as shown in figure 4.4a. Steps one and two are the cleaning of the silicon substrate and the coating of the substrate with CTF-1 solution, respectively, air-drying for at least 12

hours. After that, the sample was coated with two polymer layers: lift-off resist (PMMA) and thermal resist (PPA) by spin coating. The details in the desired shape are imprinted onto the PPA layer using the NanoFrazor. The lift-off resist is subsequently removed by wet chemistry, generally a base, and this provides for an isotropic etch process with the resultant undercut profile. Then a thin layer of material is usually deposited, generally by evaporation. Finally, the pattern is immersed in a solvent to remove both the lift-off resist and the PPA, along with excess deposited material. The process serves to effectively transfer the pattern from the PPA to the deposited material.



(a) Bilayer lift-off process.



(b) Side illustration of Bilayer lift-off process.

Figure 4.4: Illustration of Bilayer lift-off Process for device fabrication

Some key points to consider when choosing the right process were that we wanted to pattern an evaporated thin film and that the smallest features of our pattern were larger than 100nm.

4.6.1 Substrate preparation and resist coating

The silicon substrate was first sonicated for 5 minutes in acetone, followed by 5 minutes in isopropyl alcohol and then 5 minutes in deionised water; the substrate was then blown dry with nitrogen gas.

After cleaning, the solution was dropped onto the substrate and air-dried for 24 hours. Once the substrate was dry, a lift-off resist (PMMA) and a thermal resist (PPA) were drop-cast in a spin coater.

In general, the thickness of a film produced by spin coating is inversely related to the square root of the spin speed, as described by the following equation, where t represents the thickness and ω denotes the angular velocity in revolutions per minute (rpm):

$$t \propto \frac{1}{\sqrt{\omega}} \tag{4.1}$$

According to eq. 4.1, increasing the spin speed by a factor of four results in a film thickness that is reduced by half. The required thicknesses for the PMMA (100 nm) and PPA (120 nm) layers were determined based on a combination of the spin speed tables provided in the NanoFrazor recipe book (version 3.2 / 01 2024) [**Nanofrazor**] (see Table 4.1 and Table 4.2) and experimental data from prior work conducted by a former lab member, who had previously utilized these materials on the same substrates, for different materials and approaches different thicknesses may be used [57, 12, 2].

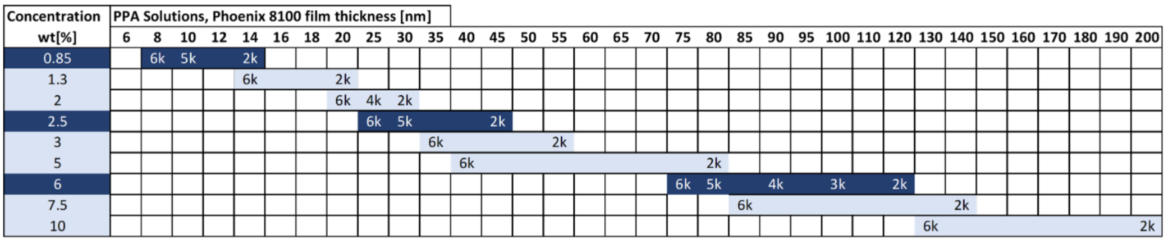
To create the PMMA layer, a solution of PMMA/MA 617.03 was used; then the film was spun at a speed of 4K rpm and then subjected to a 90-second bake on a hot plate set to 180°C.

Next, a 6 wt [%] PPA solution was applied by spin coating at 2K rpm, followed by another bake on a hot plate at 110°C for 60 seconds.

Table 4.1: Spin-speeds and dilutions of PMMA/MA AR-P 617 required to achieve various film thicknesses.

Resist thickness [nm]	Spin speed [rpm]		
Solution	2k	4k	6k
PMMA/MA 617.015	50	40	35
PMMA/MA 617.02	70	50	45
PMMA/MA 617.03	140	100	90
PMMA/MA 617.04	220	155	140
PMMA/MA 617.045	250	180	160
PMMA/MA 617.06	400	285	250

Table 4.2: Spin-speeds and concentrations required to achieve various thicknesses of PPA using Phoenix 8100 from Allresist.



Concentration	PPA Solutions, Phoenix 8100 film thickness [nm]																																	
wt[%]	6	8	10	12	14	16	18	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95	100	110	120	130	140	150	160	170	180	190	200
0.85		6k	5k		2k																													
1.3					6k			2k																										
2								6k	4k	2k																								
2.5									6k	5k			2k																					
3											6k				2k																			
5												6k								2k														
6																			6k	5k		4k		3k		2k								
7.5																					6k							2k						
10																											6k							2k

4.6.2 Patterning

The subsequent process was patterning. The latest in nanofabrication techniques is called thermal scanning probe lithography (t-SPL), which deals with nanopatterning ability, both chemical and physical, on miscellaneous materials and polymer resists. The resolution can reach up to approximately 10 nm on the lateral side and depth as fine as 1 nm [58]. This offers unusually high resolution and most of the attention in advanced materials science and microfabrication technologies today.

NanoFrazor

The NanoFrazor Explore is the first commercial t-SPL system. The sharp tip of the nanolithography tool carefully sculpts the resist material on a surface to achieve nanostructures of very good resolution. This technique is very crucial for the development of nanostructures in various applications, including electronics, due to its exceptional performance in nanopatterning [**Nanofrazor**].

The NanoFrazor operates in a closed-loop operational state (see Fig. 4.5), which constantly updates itself through optimisation based on a feedback system. Hence, very high

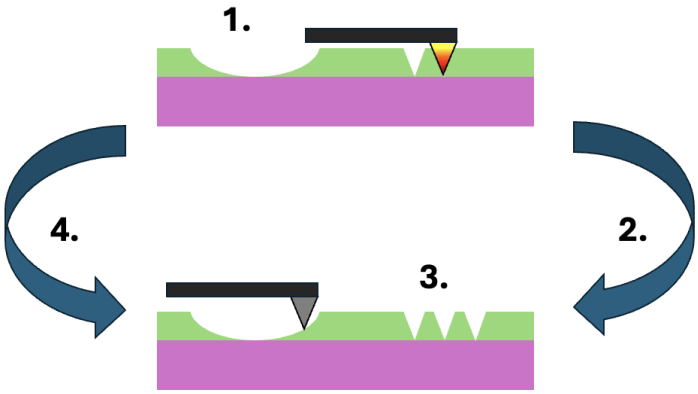


Figure 4.5: NanoFrazor's closed loop operation.

accuracy, reliability, and reproducibility of the results in the patterning process are guaranteed [**Nanofrazor**].

Fig. 4.5 shows the millisecond process followed to create this closed loop.

Step 1. The NanoFrazor patterns one line using the hot tip

Step 2. The Tip cools down in few microseconds.

Step 3. We receive an image topography of written line.

Step 4. We receive a feedback algorithm to adapt patterning.

4.6.3 Ethanol Etch

After patterning on PPA, the PMMA / MA AR-P 617 layer was dissolved using a solution of deionised water (DIW) and isopropanol (IPA). The development rate of this process depends on the concentration of DIW in the solution. To achieve a development rate of approximately 1 nm/s, a mixture containing 5 v-% DIW in IPA (e.g. 2.5 ml DIW with 47.5 ml IPA) was used.

Chapter 5

Results and Discussion

5.1 Material's characteristics

As mentioned above, CTF-1 showed promising properties which indicated it could have a potentially high electron mobility, making it a promising prospect for the fabrication of a 2D FET. It can be seen in Fig. 5.1 that the absorption spectrum starts with a high value around 200-300 nm and then decreases as the wavelength increases. This is fairly typical for many organic materials (as can be seen in Fig. 2.11 from [53]), where the higher energy UV light is absorbed due to electronic transitions within the material. It appears that absorbance decreases slightly with time, especially in the first days, for example, 18 June, compared to 21 June and 19 June. In terms of later dates, the differences in the spectra tend to be less intense, indicating that the absorbance of the material stabilises with time. The shapes of the spectra are also in such a way that no major shifts in the peaks denote that the basic electronic structure of the material has not varied much.

The slight decrease in absorbance over time may indicate some degradation or a change in the dispersion of the material in the solvent. This is common with sonicated samples [59], where the initial high-energy input can create a stable state that evolves slowly. The decrease in absorbance may also indicate that the material is aggregating or settling over time. This can often be seen when particles begin to clump together, reducing the effective surface area and thus the absorbance.

On 24 July the spectrum appears to stabilise, indicating that whatever changes have occurred have reached equilibrium. This could mean that the material is now in its most

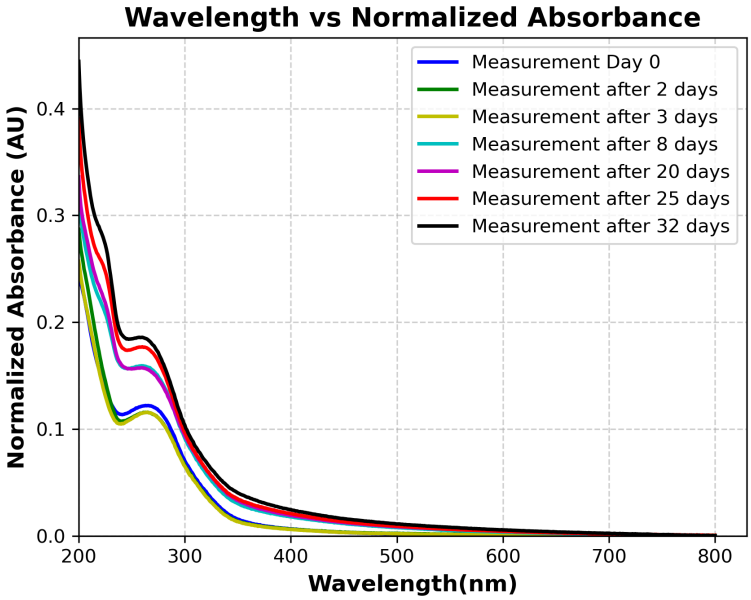


Figure 5.1: Normalized absorbance for CTF-1 solution.

stable form.

The thickness of this sample has been measured using atomic force microscopy to analyse (AFM) the structural characteristics in a high-resolution manner. The first AFM scans (performed when the solution was first synthesised) shown in Fig. 5.2 show a high-resolution topographic profile of the surface. As we can clearly see from Fig. 5.2, the scans indicate that the material thickness is within 2-3 nm, at the level of two atomic layers. This thickness agrees with expectations for a bilayer structure and is in good accordance with the intended design of this material, confirming that it is thin in some places.

A later performed AFM analysis, shown in Fig. 5.3, shows thickness variability across the sample. In the 3D topography map, it can be noticed that there are areas with considerably higher thickness, up to approximately 347.6 nm. The difference in thickness between the original 2D scan and this later 3D topography measurement in the AFM provides evidence of a much more complex surface morphology.

There are a number of factors that could cause this increase in the observed thickness: possible additional layers or aggregations of the material as it ages can form localised areas where the material is much thicker. In addition, the surface roughness observed in 3D topographies may indicate surface contamination, incomplete layer formation, or defects introduced during sample preparation or during the deposition of the material.

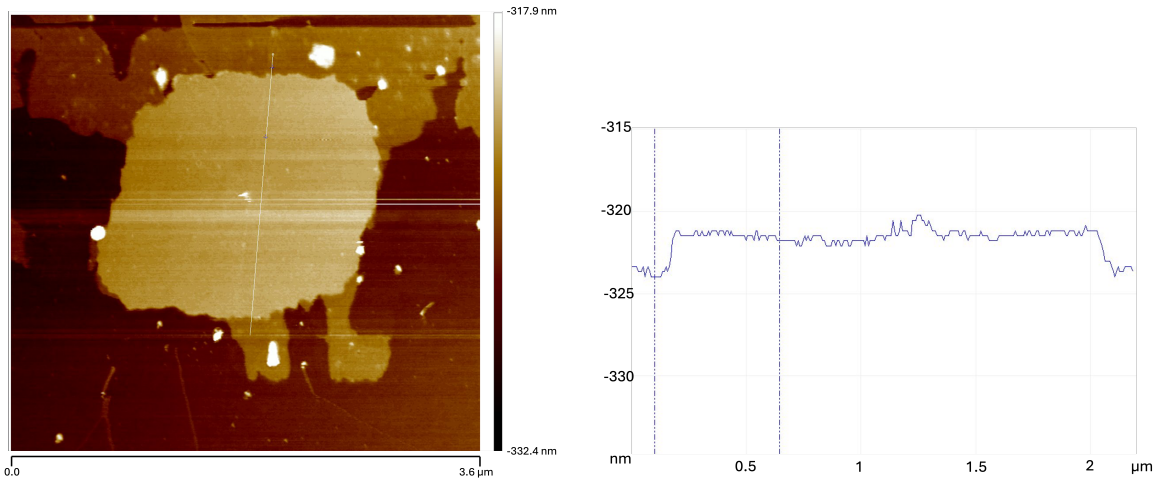


Figure 5.2: Atomic Force Microscope Analysis of the sample when it was synthesised. Images were processed by Gwyddion.

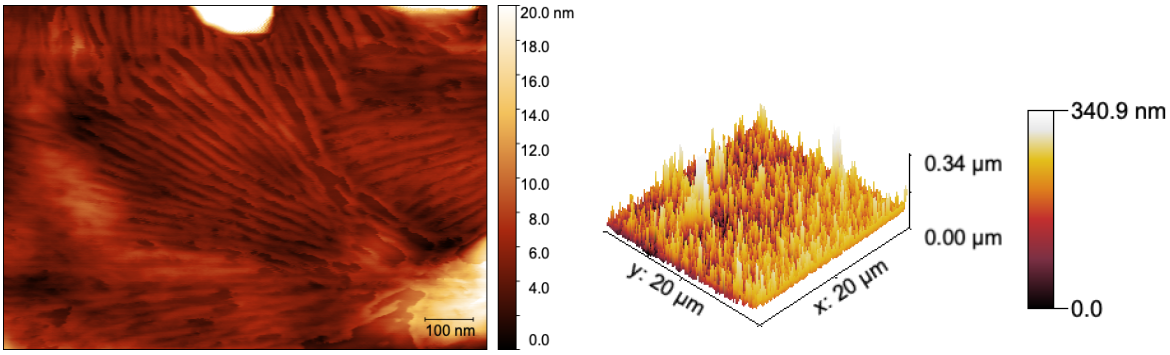


Figure 5.3: Atomic Force Microscope Analysis of the sample 16 months after synthesis. Images were processed by Gwyddion.

5.2 Sample 1. Device fabricated by depositing different concentrations of CTF-1 solution in silicon dioxide (SiO_2) with interdigitated electrodes

The purpose of this step was to determine the most suitable concentration for device fabrication, based on the uniformity and quality of the deposited layers as well as their interaction with the electrodes. The images of the devices coated with different concentrations can be seen in Fig. 5.11

In Fig. 5.4, it can be seen that the current ranges from -10 to 10 mA. The value is a relatively high current level, suggesting significant charge transport; compared to the current seen in Fig. 5.5, where the current ranges from -.02nA to .02nA, which is much lower than the device coated with C_1. This implies that the device is much less conductive, suggesting

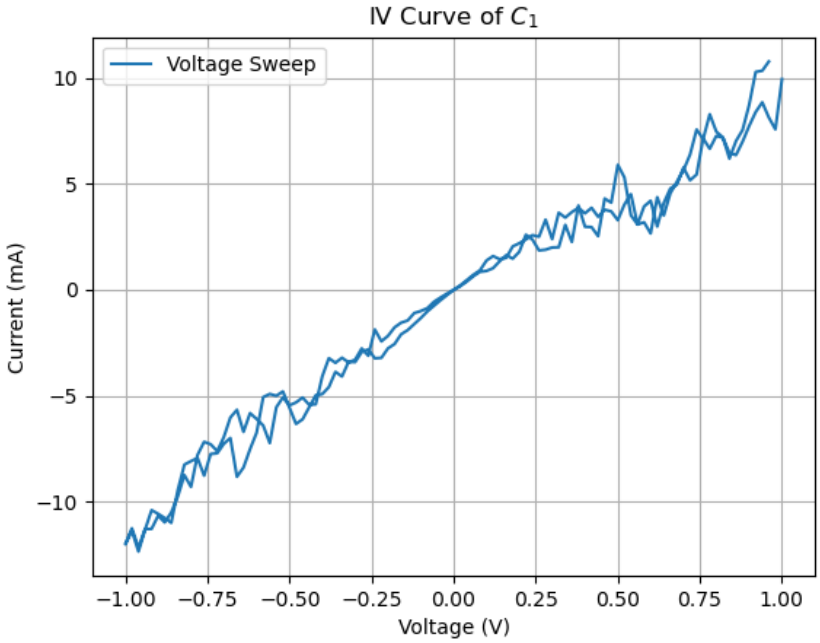


Figure 5.4: IV Curve for Device coated with Concentration C_1.

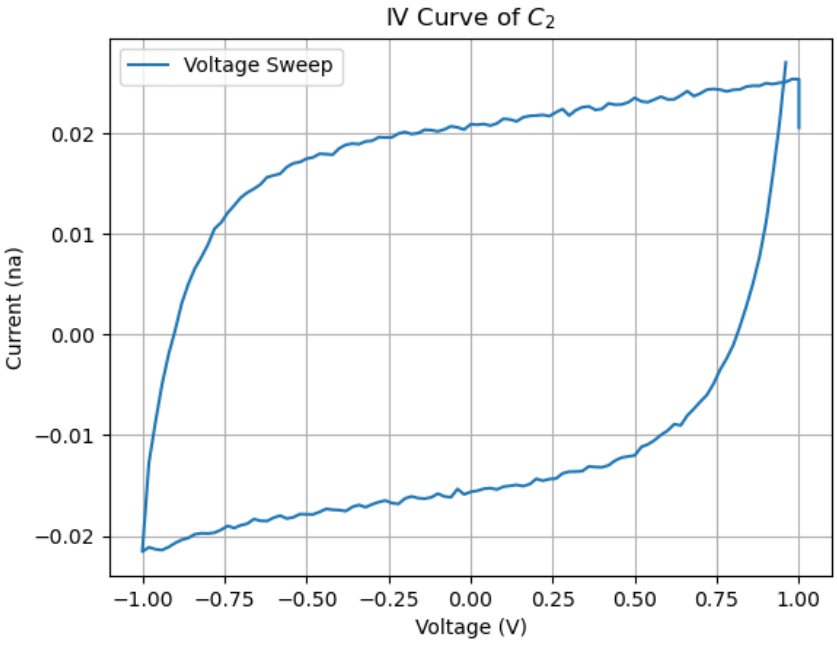
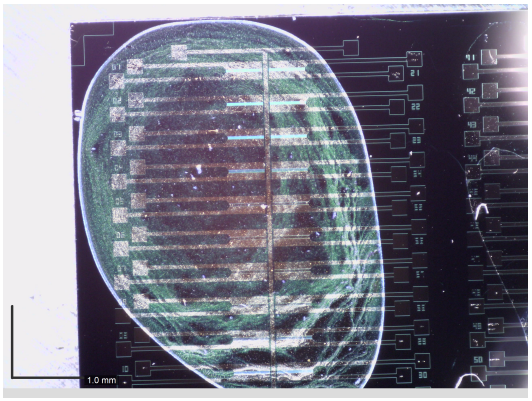


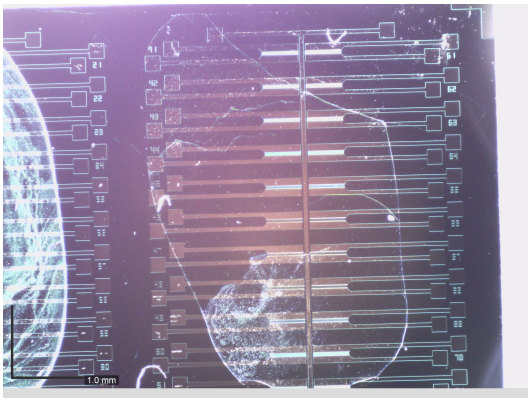
Figure 5.5: IV Curve for Device coated with Concentration C_2.

that the device with C_1 (a higher concentration of CTF-1) shows stronger conductivity.

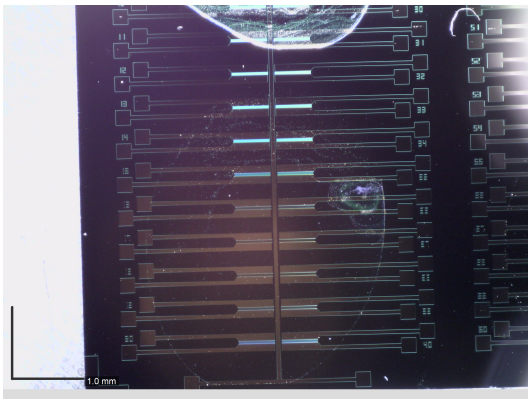
The same behaviour was observed with lower concentrations C_3 and C_4. Leaving C_1 the desirable concentration.



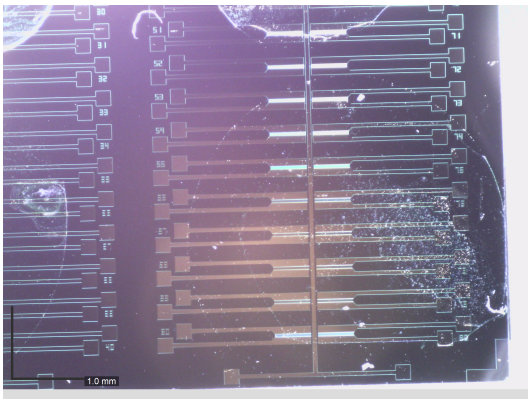
(a) Image of devices coated with 0.1 mg/mL of CTF-1. (corresponding I–V characteristics shown in Fig. 5.4)



(b) Image of devices coated with 0.0025 mg/mL of CTF-1. (corresponding I–V characteristics shown in Fig. 5.5)



(c) Image of devices coated with 0.00025 mg/mL of CTF-1.



(d) Image of devices coated with 0.000125 mg/mL of CTF-1.

Figure 5.6: Microscope images of a fabricated devices with different concentrations deposited into the interdigitated electrodes

5.3 Sample 2. Device fabrication by CTF-1 solution deposition on silicon dioxide (SiO_2) chip with interdigitated electrodes

Upon determining the ideal concentration from Sample 1, we proceeded to create a second device by applying this concentration by dropcasting it onto another chip with interdigitated electrodes. Devices coated with a higher concentration of CTF-1 show milliampere range current offering detectable charge transport, which is beneficial for experiments that require significant current flow; this being the reason why the following sample was fabricated with this concentration of CTF-1. The large surface area of the interdigitated configuration continued to offer high reliability for contact with CTF-1 flakes as it ensures that at least one of the electrodes will contain flakes of this material.

Figures 5.7 and 5.8 show the output characteristics of a MOSFET fabricated with CTF-1 as the 2D material and silicon as the substrate, measured at different gate voltages ($-40V$, $0V$ and $40V$). Data are plotted as SMU-1 current (A) versus SMU-1 voltage (V) for two voltage sweeps: from $0V$ to $-10V$ (5.7) and from $0V$ to $10V$ (5.8). In Fig. 5.7 we can see that the current increases as the voltage becomes more negative, which is typical for an N-channel MOSFET in the negative voltage range. The curve then shifts upward as the gate voltage increases from $-40V$ to $40V$, indicating improved channel conductivity at higher gate voltages. In both plots, a gate voltage of $-40V$ produces the lowest current levels, indicating reduced channel conductivity, followed by a gate voltage of $0V$ and finally a gate voltage of 40V, showing the highest current.

The use of CTF-1 as a 2D material in the MOSFET appears to affect the current-voltage characteristics, possibly contributing to the noise appearing in the graphs and the variation in current levels. The shift of the curves with the gate voltage confirms that the device operates as a MOSFET, with typical behaviour expected from the gate voltages applied.

The graph 5.9 shows the transfer characteristics of the same MOSFET device, A01, from sample 3. The transfer curve shows the relationship between the gate voltage (V_{GS}) and the drain current (I_{DS}) at a fixed drain source voltage ($10V$ in this case).

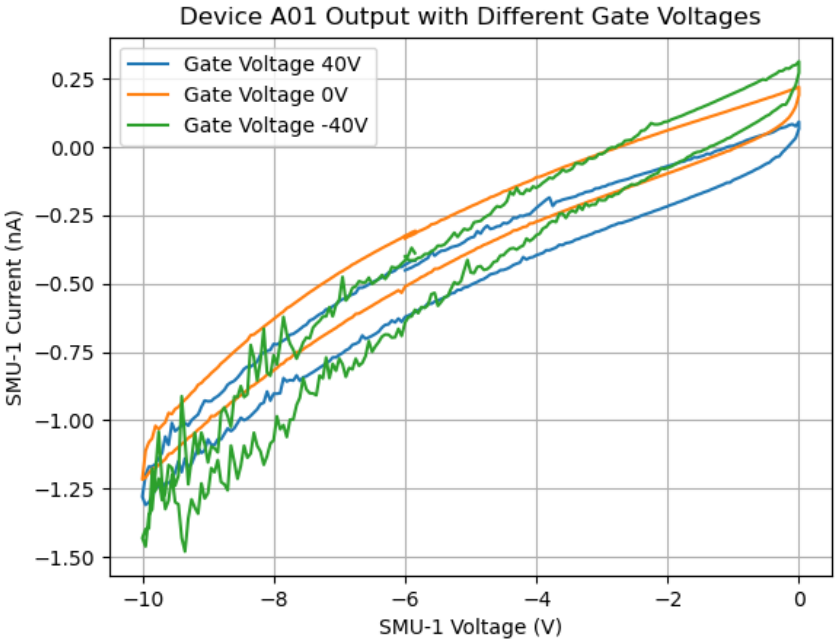


Figure 5.7: Output measurement of Device A01 from -10V to 0V at different gate voltages.

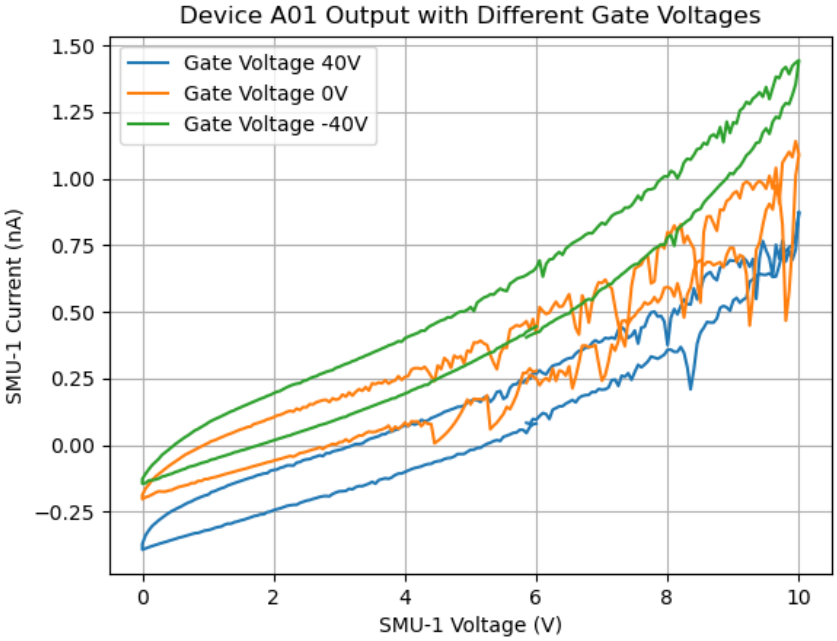


Figure 5.8: Output measurement of Device A01 from 0V to 10V at different gate voltages.

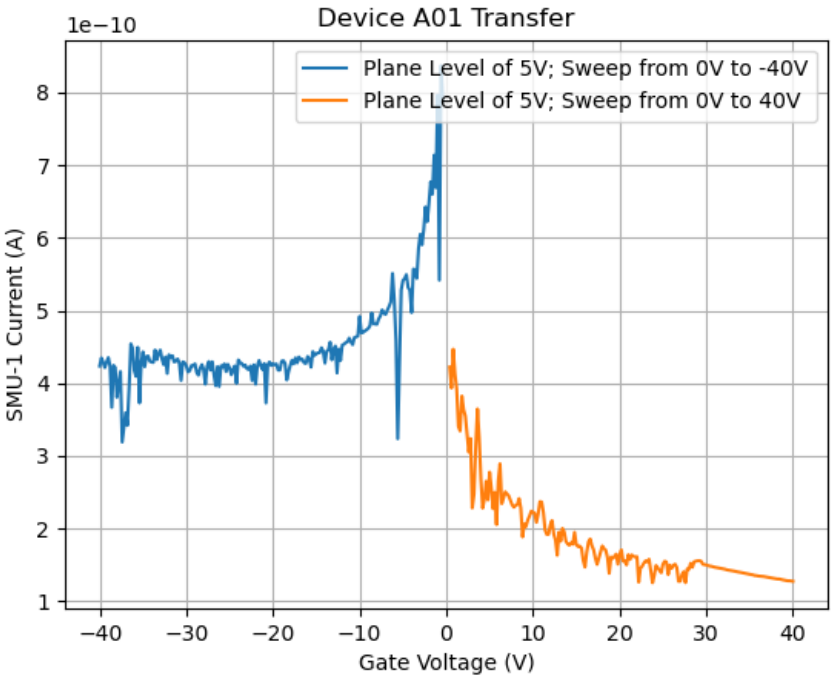


Figure 5.9: Transfer measurement of device A01 from -40V to 40V.

5.4 Sample 3. Device fabrication by CTF-1 solution deposition in silicon dioxide (SiO_2) with electrodes concentrated in a smaller area

Having obtained the optimal concentration and achieving device-like behaviour in the last sample, our objective was to minimise the surface area covered by the electrodes, while the area in the previous samples was much larger. This smaller, more concentrated electrode design aims to determine whether similar electrical behaviour could be achieved with a more focused measurement area.

The output curves shown in Fig. 5.10 show the relationship between SMU-1 voltage (V) and SMU-1 current (A) at different gate levels for different devices.

As can be seen, all the devices show exactly the same behaviour, but with slightly different values; the curves show typical output characteristics of a MOSFET, where the current (I) through the device increases as the voltage (V) across it increases. We can see that as the gate voltage (V_G) increases from $-40V$ to $40V$, the current through the device also increases, indicating that the device channel becomes more conductive as the gate voltage increases.

In addition, when the gate voltages become lower ($-40V$ and $-20V$), the SMU-1 voltage becomes more and more negative, reflecting a great increase in current. This means that, under those conditions, strong conduction is occurring within the device, probably as a result of increased attraction of carriers into the channel.

The device then enters a saturation region at higher voltages where the current levels off, indicating that the MOSFET is operating in saturation mode where the channel is pinched off and the current could be considered "constant". For positive gate voltages of $20V$ and $40V$, the curves have upward shifts, indicating that for a given SMU-1 voltage, the device current has increased. This is to say that with an increase in the gate voltage, the device conducts better current-perhaps because of better channel formation. For even higher positive gate voltages, the upward steep rise of the curves is accompanied by a decrease in saturation-a must for better channel formation.

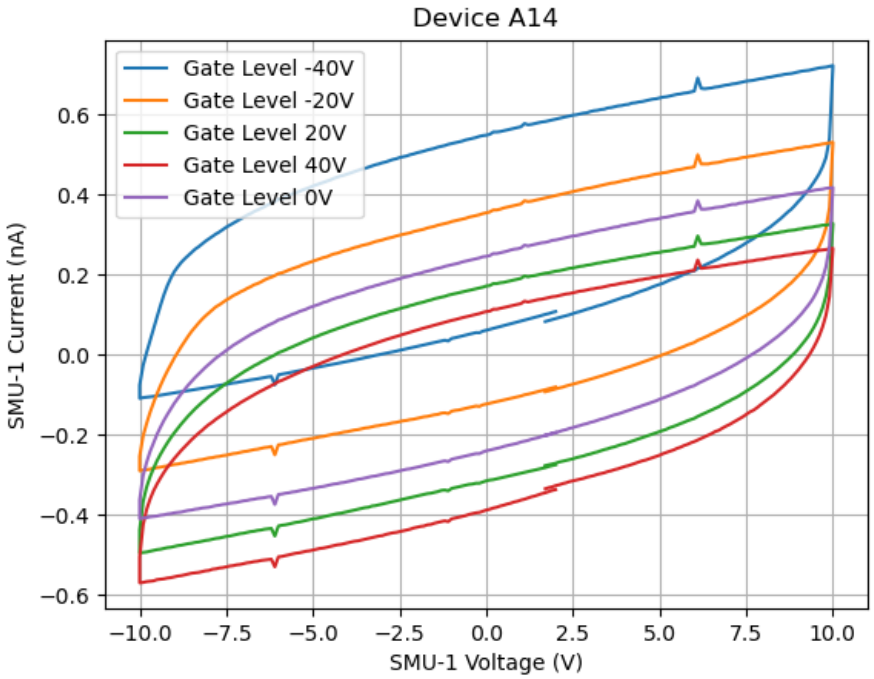
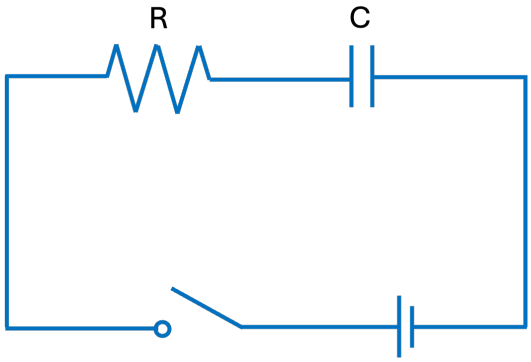


Figure 5.10: Output measurement for device A14.

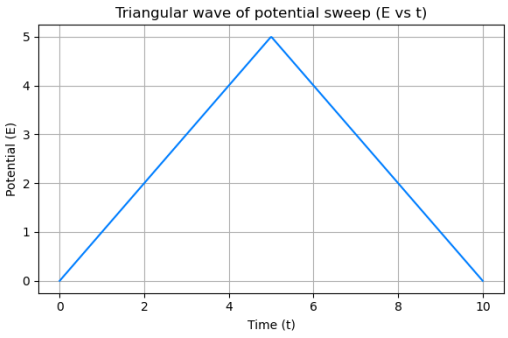
The point at which the curves begin to increase significantly from zero (at approximately $V_{SMU} = 0V$) indicates the threshold voltage at which the device begins to turn on and conduct. This threshold changes as a function of the gate voltage applied, demonstrating the gate's ability to control current flow. It is apparent that the different curves show that the behaviour of the device changes with different gate voltages, showing that the device

modulates the current properly. The layout of the curves indicates good control of the current through the device, which is an important feature for a functioning transistor.

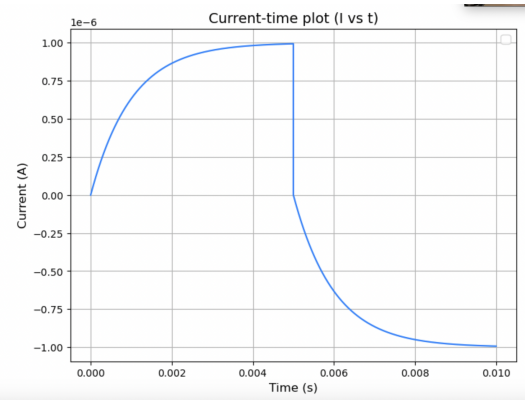
Therefore, the observed behaviour may indicate that CTF-1 has the capability to support efficient gate control, and hence provides an opportunity for the modulation of current through the device. This could mean that modulation of current may be possible in a wide range of gate voltages, which indicates good charge transportation inside the device due to CTF-1. The output characteristics present a working MOSFET that can properly switch between the on and off states.



(a) RC circuit.



(b) Triangular wave of potential sweep.



(c) Current–time.

Figure 5.11: (a) RC circuit, (b) triangular wave of potential sweep and (c) current–time.

Hysteresis may be critical in any analysis of the electrical characteristics of the device. This is especially true during cyclic voltammetry when the background current is analysed. One needs to understand from the actual reactive currents the contributions that arise because of the double-layer charging effect. Hence, the capacitance current due to the background electrolyte must be known.

An RC circuit model representation could be done by the double layer capacitance and

the solution resistance in Fig. 5.11a. It plays a significant role in developing the overall charging-discharging behaviour that, in turn, reflects itself directly into the current response whenever the potential is swept [60]. Starting from Kirchhoff's law:

$$V(t) = V_R(t) + V_C(t) \tag{5.1}$$

where, $V_R(t) = IR$, the voltage drop across the resistor is proportional to the current and $V_C(t) = \frac{Q}{C}$, the voltage drop across the capacitor is proportional to the charge stored there, where $Q = CV$

For a linearly increasing voltage (sweep) across the circuit, the following current is governed by the following equation:

$$I = C\frac{dV(t)}{dt} \tag{5.2}$$

where $\frac{dV(t)}{dt} = v$ is the constant sweep rate. Plugging this into the differential equation for charging a capacitor in an RC circuit and solving, you get the expression:

$$I = vC[1 - e^{-\frac{t}{RC}}] \tag{5.3}$$

where I is the current, v is the scan rate, C is the capacitance, and R is the resistance. This expression shows the time-dependent nature of the charging current as the potential is swept over time at a constant rate.

This charging current decays over time, reaching a steady state value dependent on the RC time constant. As illustrated in Fig. 5.11c), the current initially rises due to capacitive effects but eventually decays as the double layer charges fully. When the potential is reversed (as shown in Fig. 5.11b), the current also reverses direction. This reversal leads to the characteristic hysteresis seen in cyclic voltammetry (CV) curves, where the current at the same potential differs between the forward and reverse sweeps [61].

The equation presented in Eq. 5.3 describe how this capacitive background current depends on the scan rate v. These equations are central to understanding the hysteresis loops in CV data. With an increasing scan rate, the value of the charging current becomes more significant. Hence, a greater hysteresis is realised in current plots as a function of the potential. Indeed, this can be seen from the results presented in Fig. 5.10 where it becomes clear that there

exists a hysteresis loop when the current is plotted as a function of the potential.

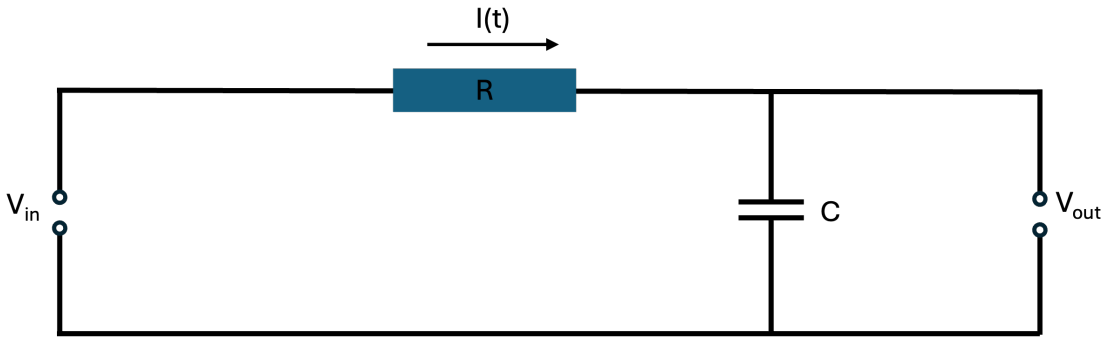


Figure 5.12: RC charging circuit.

In addition, we can analyse the circuit shown in Fig. 5.12, where V_{in} is the input voltage or the gate voltage. V_{out} is the voltage drop across the capacitor. Following Ohm's law we can say:

$$V_{out} - V_{in} = IR \tag{5.4}$$

where I is the current and R the resistance of the device. We also know that the capacitor voltage and the current flowing through the circuit is:

$$V_{out} = \frac{Q}{C} \quad \text{and} \quad I = \frac{dQ(t)}{dt} \tag{5.5}$$

substituting this into Eq. 5.4 we get:

$$\frac{Q}{C} - V_{in} = \frac{dQ(t)}{dt}R \tag{5.6}$$

Seeing that V_{in} is constant through all the experiments, we can simply rewrite:

$$\frac{Q}{C} = \frac{dQ(t)}{dt}R \tag{5.7}$$

solving for Q(t), we get:

$$Q(t) = Q_0 e^{\frac{t}{R \cdot C}} \tag{5.8}$$

Also, from Eq. 5.5, we can calculate the charge (Fig. 5.13).

As we can see, Eq. 5.8 models an RC charging circuit in which the charge on the capacitor

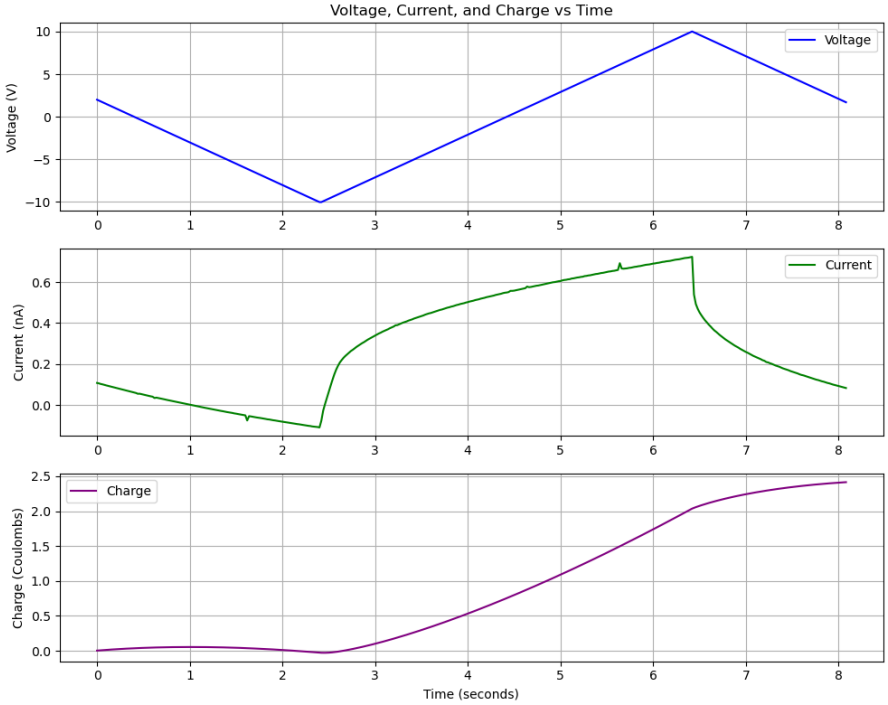


Figure 5.13: Raw Data of the device: Voltage, Current and Charge vs Time.

builds exponentially over time as current flows through a resistor into a capacitor. The shape of the curve is generally exponential, with the charge starting at a low value and increasing over time, but with a slowing growth rate as it approaches a maximum charge. Consistent with this general trend, the plot does indeed move from zero charge upward through the course of time. This would be the same shape we would expect to see in plot 5.13, as the charge starts at zero and increases over time. We can also notice that this shape of the experimental curve is more linear towards the middle and end of the plot.

Consequently, we can say that this equation partially describes the charge increase over time. The linear behaviour seen in the middle of the curve suggests that the current remains relatively stable during this period, which would result in a more linear increase in charge rather than the expected exponential growth.

However, for further analysis on the capacitance of the device, the data were averaged to remove the hysteresis and to have a clearer vision of the behaviour of the device (the analysis can be found in the appendix .1. Obtaining Fig. 5.14.

In a typical MOSFET, we would expect the gate voltage to strongly influence the current through the channel by controlling the carriers (either increasing or decreasing them). However, this does not appear to be the case in Fig. 5.14. We can also see that the conductance remains

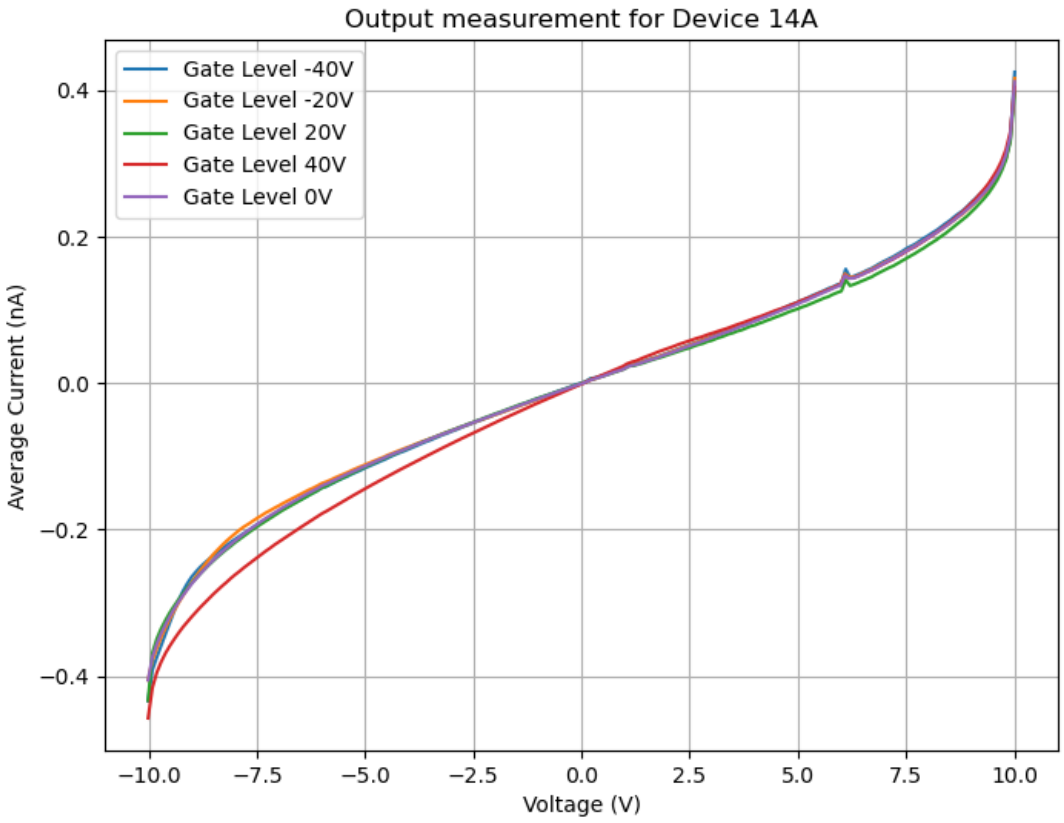


Figure 5.14: Averaged Output measurement for device A14.

almost the same across different gate voltages applied to the device. In an ideal MOSFET, we would expect an increased gate voltage to modulate the channel conductance, resulting in a higher current for the same applied voltage.

Lastly, for this sample in Fig. (5.15), we can see the relationship between the gate voltage and the current of SMU-1 over time for device A14 (5.10), with several levels of gate voltage applied ($-40V$, $-20V$, $0V$, $20V$, $40V$). The gate voltage appears to be periodically modulated, affecting the SMU-1 current. This periodic modulation could be due to an unintentional coupling effect in the device. However, when the exact same setup was tested with another device, where we knew what to expect, this dependency could not be seen. Because that gate voltage emulates the SMU-1 voltage, this could be a coupling effect or a feedback mechanism where, in fact, the gate voltage is not independent but influenced by the SMU-1 voltage. As mentioned above, CTF-1 COFs are known for their porous structure and high surface area, which can lead to significant charge trapping. Trapped charges can affect the electric field

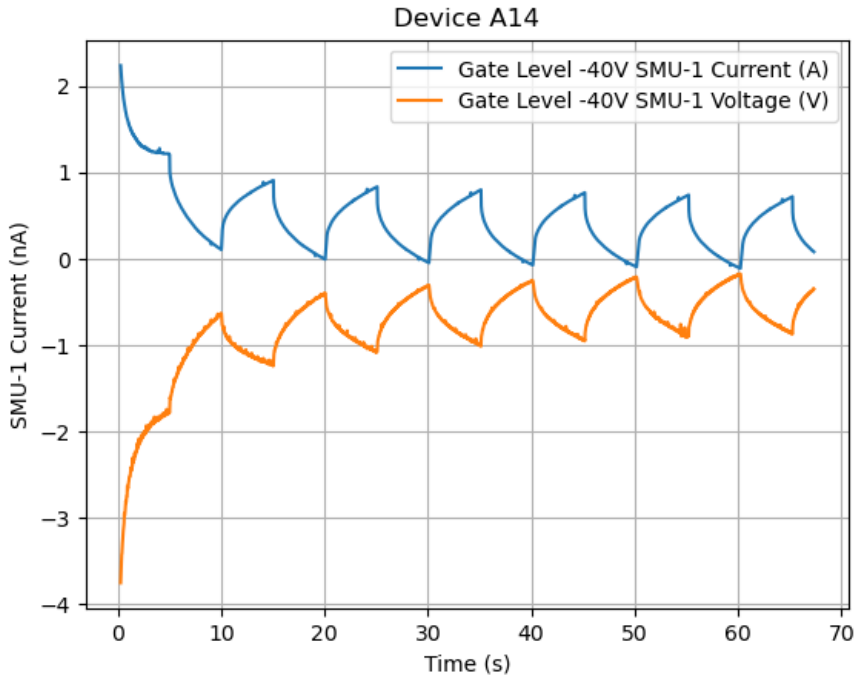


Figure 5.15: Time dependency shown between the current and gate voltage.

distribution and hence the gate voltage. Therefore, periodic modulation could be related to the time constants associated with these trapping-detrapping processes.

5.5 Sample 4. Device fabrication in silicon dioxide (SiO_2) with contact onto an individual flake of CTF-1 solution

In the final sample, the fabrication process involved depositing CTF-1 onto the chip first, followed by direct patterning of the electrodes onto a single flake of the material. This approach was adopted in an attempt to target a single, well-defined region of a material in order to improve precision in the characterisation of its electrical properties.

For the successful fabrication of the device in Figure 5.6d, it was necessary to precisely visualise the flakes in the sample during the t-SPL process. The NanoFrazor is supremely well suited for an accurate overlay of electrodes on 2D material flakes, as seen in Fig. 5.16 by the bilayer lift-off process, in this case on a MoS_2 flake [12]. This is possible, as one can easily see the topography of even materials of one atom thick under a resist stack of up to a few hundred nanometres thick [**Nanofrazor**].

However, as indicated by the previous AFM analysis, we encountered challenges in the

deposition of monolayers or bilayers, which are critical for the precise fabrication required. This difficulty is further illustrated in Fig. 5.17, where it became apparent that it was virtually impossible to locate these flakes or bulk regions within the NanoFrazor environment.

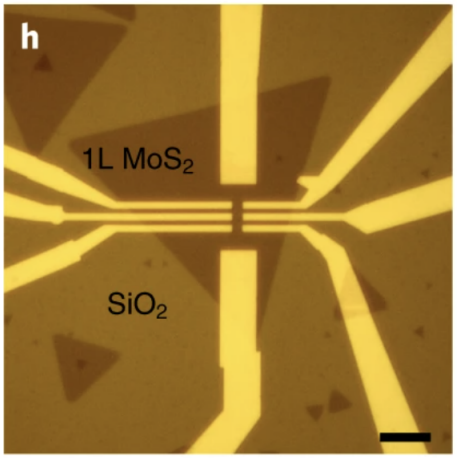


Figure 5.16: A top-gated MoS2 transistor with h-BN top-gate dielectric where all the electrodes have been patterned with the NanoFrazor. Retrieved from [12]

In spite of these challenges, we continue the process of lithography to ensure that it is possible to write on the polyphthalaldehyde surface. As can be seen in Fig. 5.18, even without having the intended flakes - probably due to the ageing of the solution- we were able to pattern well in the CTF-1-PMMA-PPA stack. Figure 5.18 shows that we were able to pattern and subsequently measure the depth of the scan, which was equal to the thickness of the PPA layer. The result is very important because it confirmed the viability of the writing on this layered stack and, therefore, could be a possibility for future device fabrication if the synthesis process was refined to produce such flakes reliably.

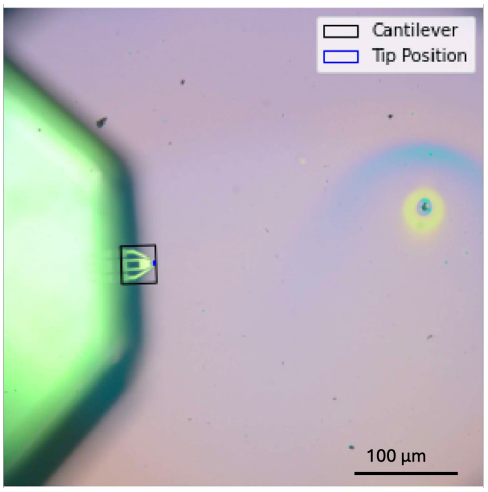


Figure 5.17: Image of the tip and cantilever of the NanoFrazor. The image shows that no flakes of CTF-1 are visible under the virtual environment. Images are screenshots from NanoFrazor Logbook.

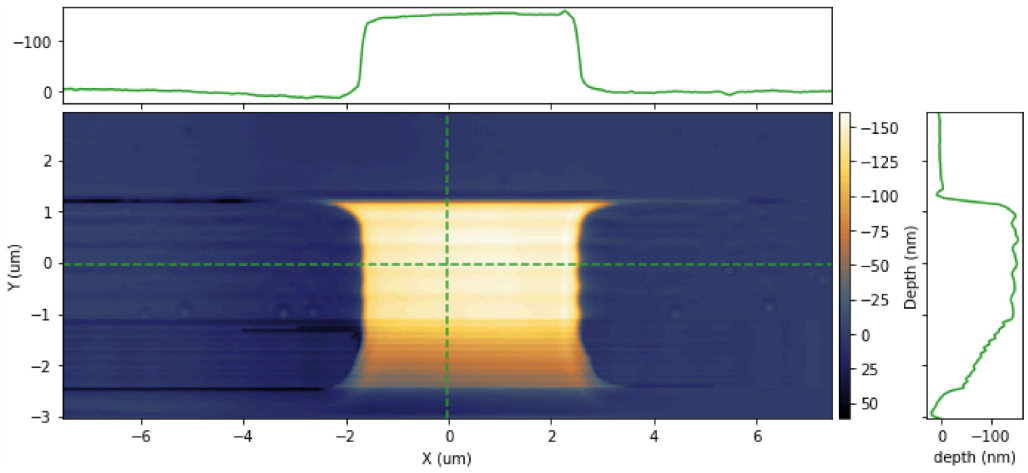


Figure 5.18: A depth profile over the edge of a patterned area on the film thickness. Image is a screenshots from NanoFrazor Logbook.

Chapter 6

Conclusions

In this project, we tested the ability to fabricate these devices using three different methods, each of which differs in the type of electrodes used or their arrangement.

6.1 Materials characteristics

The first AFM analysis performed when the solution was synthesised in fact verified the thin structure of the material in some regions, as anticipated on its surface for a bilayer thickness. However, the variation in thickness observed from the samples with time would suggest a more complicated surface morphology, which might be due to ageing, surface contamination, or defects within the preparation process. These results again point towards further refinement in the fabrication and handling processes to get consistent material characteristics throughout the sample.

6.2 Sample 1. Device fabricated by depositing different concentrations of CTF-1 solution in silicon dioxide (SiO_2) with interdigitated electrodes

The aim of this step was to identify, based on layer uniformity and quality, as well as electrode interaction, the ideal concentration to be used in device fabrication. C_1 yields higher conductivities compared to its lower concentrations, C_2, C_3 and C_4, making it highly desirable.

6.3 Sample 2. Device fabrication by CTF-1 solution deposition on silicon dioxide (SiO_2) chip with interdigitated electrodes

Using the identified optimum concentration, we successfully reproduced deposition on another chip with interdigitated electrodes. Thus, this confirms that the chosen concentration and large surface area configuration reliably capture measurable electrical properties. Typical current-voltage behaviour was observed in the MOSFET fabricated using CTF-1 as the 2D material; the conductivity of the channel improved as the gate voltage increased from -40 V to 40 V. The shift in curves signifies that the appropriate operation of the MOSFET is observed, although noise and variation in current levels were observed probably due to the properties of the CTF-1 material. Together, these results reflect that CTF-1 has the possibility of being used effectively in a MOSFET device; however, further optimisation may help to reduce noise and improve the consistency of electrical characteristics.

6.4 Sample 3. Device fabrication by CTF-1 solution deposition in silicon dioxide (SiO_2) with electrodes concentrated in a smaller area

By focussing on device fabrication in the central part of the chip, we minimised the electrode surface area. At a basic level, the output curves for sample 4 presented typical features of a MOSFET: the current that passes through a device increases with increasing gate voltages. From these values, we conclude that CTF-1 shows effective gate control, allowing modulation of current.

Nevertheless, the average data shown behave in a manner that was not expected; the conductivity was the same with the different gate voltages-a distinct contrast to typical behaviours from MOSFETs. This inconsistency could be due to some kind of coupling or feedback that involves the trapping of charge within the CTF-1 material.

However, periodic modulation in the time-dependent data can be further support of the hypothesis that charge-trapping and detrapping processes have been affecting the electric-field distribution. In other words, the basic characteristics of functional MOSFET are present, but from these results, the complex features promoted by the porous structure of CTF-1 give an

opportunity for further studies that will be targeted to optimise the performance of the device and reduce unwanted coupling effects.

6.5 Sample 4. Device fabrication in silicon dioxide (SiO_2) with contact onto an individual flake of CTF-1 solution

The last sample, with electrodes patterned directly onto a single flake of CTF-1, was particularly challenging to prepare due to the inefficiency of precisely locating monolayers or flakes along the substrate, as was noted when referring to AFM analysis. The reality of this was such that thermal scanning lithography was unable to identify desired flakes within the nanofrazor environment. Successful patterning has been achieved on the CTF-1-PMMA-PPA stack despite these problems, since depth measurements carry values that would show correspondence for a layer of PPA. We can conclude that, while much work is needed to improve material synthesis and flake deposition, the writing in this stack still remains viable and gives a promising platform for future development.

6.6 Future promises

Further research involves the reproduction of sample 4 results using single flakes or monolayers of CTF-1. Since it is already possible to pattern the stack of CTF-1-PMMA-PPA, the remaining big task is the synthesis of the CTF-1 solution producing single flakes or monolayers. It also remains important to understand the time-dependent charge behaviour within the device to ensure its capability in the real world. Indeed, the RC charging equation is a brilliant model explaining the charging and discharging processes in MOSFET devices, however, real-world phenomena such as charge trapping and stable current flow can lead to deviations from the ideal behaviour.

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Chapter 7

Appendices

.1 Average for Output Measurements

.1.1 Raw Data

First, we graph the raw date of the voltage versus the current. The raw data plot can serve to visualise the structure of the voltage and current over the course of the experiment, making more evident how to identify patterns such as start and end points of the sweep. That way, it is easy to see where the voltage begins to increase (upward sweep) and where it begins to decrease (downward sweep) [60].

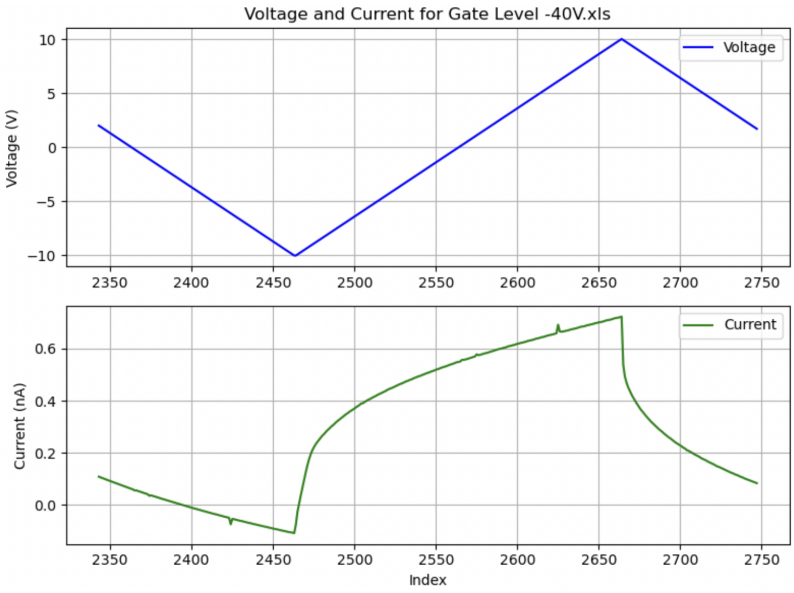


Figure 1: Raw Data for Voltage and Current.

Graphing voltage against index provides a clear distinction between the upward and

downward sweeps. The boundaries across the sweeps are the voltage transitions where the record begins to rise and descends.

.1.2 Identifying the sweeps

After identifying the behaviour of the data, we can identify the sweep:

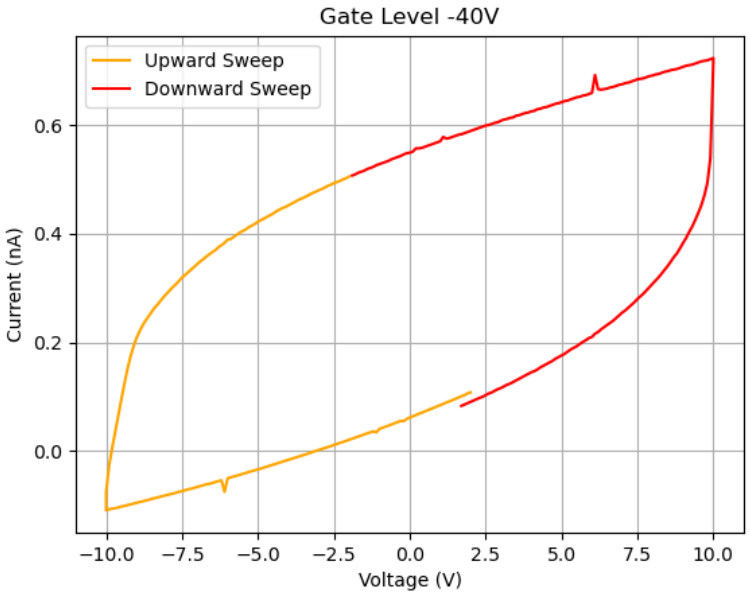


Figure 2: Upward and Downward sweeps.

.1.3 Averaging the plot

Finally, now that the sweeps have been identified, we can begin to average the plots.

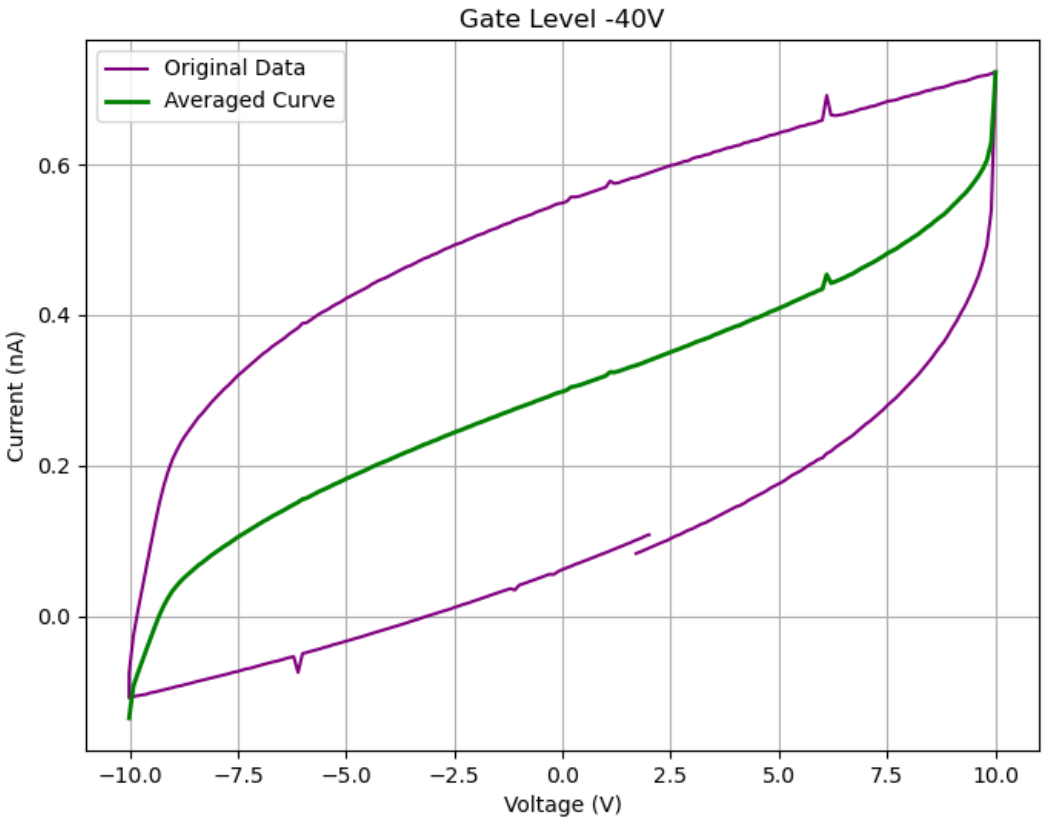
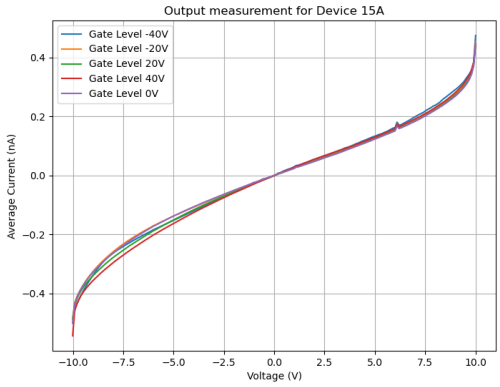


Figure 3: Averaged Output of Device A14 for Gate Level at -40V.

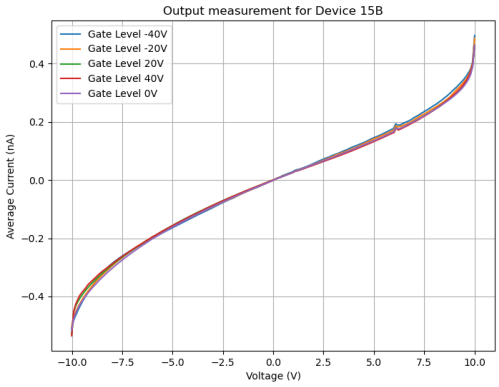
.2 Other Device results for sample 4. Device fabrication by CTF-1 solution deposition in silicon dioxide (SiO2)

In the present appendix, we report the I-V characteristic of the devices tested by applying the same measurement methodology followed during sample 4. The plots show typical current versus voltage behaviour at different gate voltage settings.

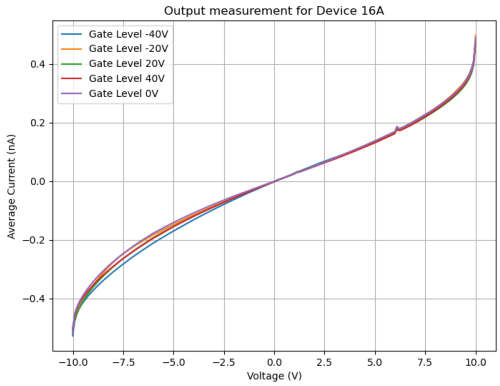
Devices 15A, 15B, 15A, 16B, 17A, and 17B behave similarly with Sample 4 wherein the variations in gate voltage do not fundamentally affect the general relationship of current to voltage. The curves for different gate voltages lie practically on top of one another since at this point, the device operates in the saturation region wherein the drain current becomes independent with further increase in the gate voltage.



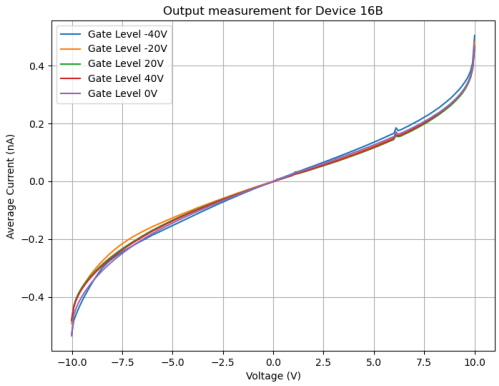
(a) Averaged Output measurement for device 15A.



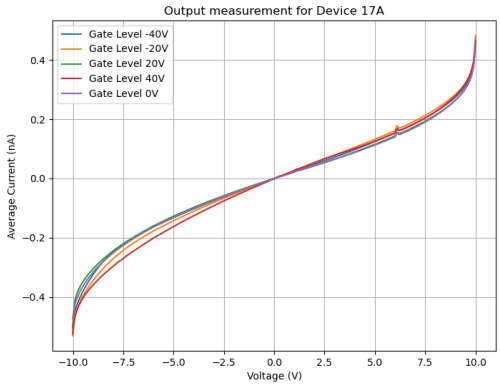
(b) Averaged Output measurement for device 15B.



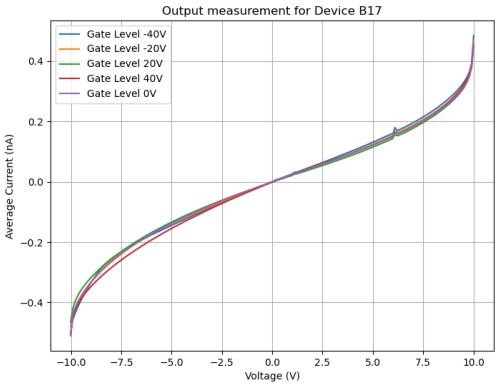
(c) Averaged Output measurement for device 16A.



(d) Averaged Output measurement for device 16B.



(e) Averaged Output measurement for device 17A.



(f) Averaged Output measurement for device 17B.